آگهی فراخوان شناسایی ۱۰/۱۴۰۳/۰۰۱

شرکت پتروشیمی اروند (سهامی عام) در نظر دارد نسبت به شناسایی شرکتهای سازنده داخلی و توانمند برای ساخت انواع کارت های الکترونیکی و ماژول های مربوط به PLC های یکسوساز این شرکت، مطابق با مشخصات مندرج (فایل پیوست) به شرح ذیل اقدام نماید:

۱) SPU۲۳۲,۱-CAN
۲) DEP ۲۳۲,۱
۳) DAP ۲۳۲,۱
۴) ADA ۲۳۲,۱

لذا از شرکت‌های سازنده فعال در این زمینه دعوت می‌شود اسناد و مدارک ذیل را حداکثر تا ساعت ۱۲:۰۰ روز دوشنبه مورخ ۱۴۰۳/۰۲/۱۷ به نشانی استان خوزستان – بندر امام خمینی – منطقه ویژه اقتصادی پتروشیمی- سایت ۳ – کد پستی ۶۳۵۶۱۷۸۷۳۴ امور حقوقی و پیمانها شرکت پتروشیمی اروند تحویل نمایند:

الف- اساسنامه، آگهی تاسیس، پروانه فعالیت
ب- معرفی کارخانه یا کارگاه
پ- سوابق اجرایی کار مشابه یا مرتبط با ذکر مبالغ قرارداد
ت- رزومه علمی و فنی پرسنل
ث- سوابق گواهی حسن انجام کار مشابه یا مرتبط با کار
ج- معرفی نفرات فنی به همراه لیست تایید شده اداره بیمه
چ-ارائه لیست دستگاه و ماشین آلات
خ-ارائه گواهینامه های ایزو با کد رهگیری

۱) بر روی پاکت ارسال مدارک، موضوع و شماره فراخوان مندرج گردد.
۲) به پاکت‌های ارسالی که پس از تاریخ مندرج در آگهی تحویل گردد؛ ترتیب اثر داده نخواهد شد.
۳) متقاضیان در صورت نیاز به اطلاعات فنی بیشتر میتوانند با شماره تلفن: ۰۶۱۵۲۱۲۶۶۰۰ و جهت اطلاعات حقوقی با تلفن: ۰۶۱۵۲۱۲۶۴۷۴ تماس حاصل نمایند.
۴) تصویرآگهی به همراه شرح مختصر کار از طریق نشانی اینترنتی www.arvandpvc.ir قابل ملاحظه می‌باشد.
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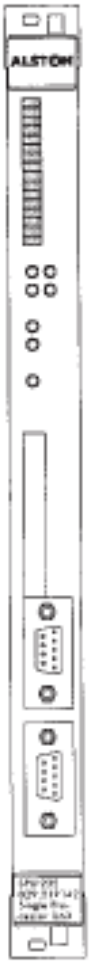
ALSTOM

SPU 232
Processor Board

Article No. 029.219142 (SPU 232)
Article No. 029.219153 (SPU 232-CAN)



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Scope of validity:

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Revision state

Rev.	Pages concerned	Remarks	Date	Designed Dept. / Name	Reviewed Dept. / Name	Approved Dept. / Name
00	all	new	10/99	E44 Klopsch	E45 Behrendt	E4 Dr. Groschupf
01	21	adapter cable	01/00	E44 Klopsch	E45 Behrendt	E4 Dr. Groschupf
02	all	SPU232-CAN	07/02	CS8 Bothe	PI421 Behrendt	PI41 Dr. Groschupf

CONTENTS

1 General

The processor board SPU 232 is a VMEbus component which is particularly suitable for executing fast control algorithms. The SPU 232 is a processor board, similar to the COP 232.1. In conjunction with other boards, the SPU 232 is capable of processing control loops via the VMEbus with polling times as short as t = 1 ms. Both Logidyn D2 applications and standard-language programs can be executed by the board. Processing rate for PI controllers programmed with LogiCAD is in the order of t = 20 µs and for a mix of approx. 100 control "blocks" in the order of t = 1.2 ms.

The board is solely designed for implementing a monoprocessor system in the DPU.1, DPU-K or DPU-S subrack. Thanks to the omission of the VME Configuration Manager Master (VCM 232.1), this board enables the cost-effective solution for small to medium-sized automation systems. The SPU 232 must always be installed in slot 0 of the master subrack, and also holds the hardware configuration of the configuration prepared using LogiCAD. It is not possible to use further, active processor and communication boards (COP 232, CCU 232, CCU 231, KPE 232, MPC 232, etc.) or expansion subracks. Connection to the **E**ngineering **N**etwork **S**ytem (ENS) is possible via the serial interfaces and COMSERVER as option.

The SPU 232 is a plug-in type VMEbus board (32-bit address and 32-bit data bus interface) of double standard Euroformat size (6 HE - height units) and a width of 4 TE (divisions).

Note: The SPU 232 board exists in two version which only differ in case of the communication interfaces. The SPU 232 board (Article No. 029.219142) as standard version is equipped with two serial interfaces, while the SPU 232-CAN board (Article No. 029.219153) has one serial and one CANbus-interface.

2 Functional Description

2.1 Processor

The AMD 5 x 86-133 or a comparable processor is used as the main processor with the following characteristics:

- internally 64-bit data bus, externally 32-bit data bus
- 32-bit address bus
- integrated L1 cache memory 16 Kbytes with write-back
- integrated floating-point processor

internal clock frequency f = 100 MHz.

2.2 Local Memories

The memories described in the following are addressed as follows:

Memory	Addresses	
Main memory DRAM 2 Mbytes, addressable 512k x 32	0000 0000H ⋮ 001F FFFFH	2 Mbytes
	0020 0000H ⋮ 00FF FFFFH	reserved
Flash disk 4 Mbytes	FF06 0000H ⋮ FF06 03FFH	1 k, register for sector address
	FF07 0000H ⋮ FF07 03FFH	1 k, data
SRAM 96 Kbytes with buffer battery	FF10 0000H ⋮ FF11 7FFFH	96 k
Bit track memory with buffer battery	FF00 0000 H ⋮ FF00 7FFF H	32 Kbytes for packed bit fields
	FF08 0000 H ⋮ FF08 FFFF H	256 Kbytes for single-bit read out, valent
	FF0C 0000 H ⋮ FF0F FFFF H	256 Kbytes for single-bit read out, antivalent
Boot EPROM 64 Kbytes	FFFF 0000H ⋮ FFFF FFFFH	64 Kbytes

- **Main Memory**

The SPU 232 comes with a 2-MByte DRAM (512k x 32 Bit) as its main memory for the general storage of data and for program execution.

The memory is **not** battery-backed.

Addressing the main memory:

0000 0000 H ⋮ 001F FFFF H	512 k x 32 = 2 MByte
0020 0000 H ⋮ 00FF FFFFH	Reserved for main memory expansion

- **Flash Disk**

The SPU 232 is fitted with a 4-MByte flash disk. It is used for non-volatile storage of the operating system and the user program (see para. 3).

The dialog control of the flash disk is designed in such a manner that access (read/write) can be carried out in the same way as with a harddisk drive; this means that it does not depend on details such as resetting the memory before writing data or special programming of a flash memory.

The flash disk is organized in blocks (sectors) of 512 bytes each. This means that 512 bytes are read or stored during each data exchange where the dialog can be organized on an 8-bit or 16-bit basis.

Dialog addresses:

Register for sector address	FF06 0000 H ⋮ FF06 03FF H
Data	FF07 0000 H ⋮ FF07 03FF H

- **SRAM**

The SPU 232 includes a battery-backed SRAM with 96 Kbytes to which the SPU 232 has a read and write access.

The SRAM-buffering is done via X1:b31, VSTDBY (VMEbus board J1) in the DPU.1 or DPU-K subrack. In order to protect the data in the SRAM, even during short interruptions in VSTDBY (battery change in the DPU.1 or DPU-K subrack or board exchange) or in case of the use of a DPU-S subrack, the SPU 232 is fitted with a lithium battery (type CR 1/3 N, Varta) which supplies the SRAM for a period of $t \geq 4$ years (at 25 °C) without data loss. If the lithium battery must be replaced, this must be completed within a time of 5 seconds in order to avoid loss of data.

Address range:	FF10 0000 H ⋮ FF11 7FFF H	96 Kbytes SRAM

- **Bit Track Memory**

In order to permit the fast processing of logic functions (control tasks), the SPU 232 is fitted with a battery-backed bit track memory for the storage of logic variables.
The bit track memory is backed by the same battery as the SRAM.

The bit track memory can be reached under three different address areas, i.e.:

- The first address area with a size of 32 Kbytes can be used for the direct writing of "packed" bit fields into the bit track memory and for the direct writing of such packed bit fields from the bit track memory. This area is, for instance, used to load the current states of digital input boards into the bit track memory.
- In the second address area with a size of 256 Kbytes, the bits entered (valent) can be read out. The individual bit is always output via data bit **D0** , whilst the data bits **D1 ... D7** are output as a defined 0-signal. This approach means faster logic operations because the processor can access all bits with direct addressing.
- In the third address area with a size of 256 Kbytes, the bits entered (antivalent) can be read out in inverted form. The inverted, individual bit is always output via data bit **D0** , whilst the data bits **D1 ... D7** are output as a defined 0-signal. This approach also means faster logic operations because the processor can access all bits with direct addressing.

Address range:	FF00 0000 H ⋮ FF00 7FFF H	32 Kbytes for packed bit fields
	FF08 0000 H ⋮ FF08 FFFF H	256 Kbytes for single-bit access, valent
	FF0C 0000 H ⋮ FF0F FFFF H	256 Kbytes for single-bit access, antivalent

- **Boot EPROM**

The boot EPROM is a non-volatile, fixed-value memory with a size of 64 Kbytes which is programmed by the manufacturer. After the connection of the supply voltage for the SPU 232 or after a reset, the boot EPROM (*Bootstrap Loader*) starts the self-test of the board and organizes the download of the user program from the flash disk into the main memory and the subsequent system start.

Address range: FFFF 0000 H
⋮
FFFF FFFF H

- **Status Register**

The SPU 232 has two status register which contains various messages of the board. It is also possible to poll the control elements (switching sockets) and to control LEDs via the software (depending on the internal program status) via the status register 1.

Status register 1

D 31	**D 30**	**D 29**	**D 28**	**D 27**	**D 26**	**D 25**	**D 24**
V3	V2	V1	V0	CFS	WrEn	CD2	0
D 23	**D 22**	**D 21**	**D 20**	**D 19**	**D 18**	**D 17**	**D 16**
MN1	MN0	SN4	SN3	SN2	SN1	SN0	0
D 15	**D 14**	**D 13**	**D 12**	**D 11**	**D 10**	**D 9**	**D 8**
Stat3	Stat2	Stat1	CD1	1	1	DPG1	DPG0
D 7	**D 6**	**D 5**	**D 4**	**D 3**	**D 2**	**D 1**	**D 0**
Error	Run	Diag	User2	User1	Quit	BatOk	SynOk

V3 ... V0			Version of the board	(read only)
CFS:	1	=	Compact flash disk inserted	(read only)
WrEn:			Software function (s. following table)	(read only)
CD2:	0	=	Flash disk ready	(read only)
MN1/MN0:			Board selection (binary coded)	(read only)
SN4 ... SN0:			Location addressing (binary coded)	(read only)
Stat3 ... Stat1:			Software function (s. following table)	(read only)
CD1:	0	=	Flash disk available	(read only)
DPG1/DPG0:	1	=	LCA loaded (**L**ogic **C**ell **A**rray)	(read only)
LCA1/LCA0:	1	=	LCA ready	(read only)
Error:			Software function (s. following table)	(read/write)
Run:			Software function (s. following table)	(read/write)
Diag:			Software function (s. following table)	(read/write)
User2/User1:			Software function (s. following table)	(read/write)
Quit:			Software function (s. following table)	(read only)
BatOk:	1	=	External battery voltage (STDBY) available	(read only)
SynOk:	1	=	External SYNC* clock available	(read only)

Name	Description	Register access	Software function	
			Self-test	Operation
WrEn	1 = pin in switching socket 319	read only	Start inhibit for MMT4	-----
Stat3	1 = pin in switching socket 121	read only	-----	Start inhibit for user program
Stat2	1 = pin in switching socket 321	read only	-----	-----
Stat1	1 = pin in switching socket 119	read only	Suppresses memory test	-----
Error	1 = LED 103B on	read/write	Hardware error	Exception
Run	1 = LED 107B on	read/write	Self-test code	Parametrization active
Diag	1 = LED 115B on	read/write	Self-test code	-----
User 2	1 = LED 107A on	read/write	Self-test code	Timeout during polling for Logidyn D2
User 1	1 = LED 109B on	read/write	Self-test code	Logidyn D2 running
Quit	1 = pin in switching socket 125	read only	-----	-----

Address for status register 1 5000 H (I/O)

Status Register 2

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
TM	EMV1	EMV0	x	0	BerrE	0	EnExt

TM: 0 = Testmode jumper inserted
EMV0: 1 = Fault level 1 exceeded (see para. 2.13)
EMV1: 1 = Fault level 2 exceeded (see para. 2.13)
x: no function
BerrE: no function
EnExt: no function

Address for status register 2 4000 H (I/O)

2.3 Timers

The SPU 232 comes with six timers:

- two free timers which can be used for "prompt" signals,
- one timer used by the operating system MMT4,
- one timer for the generating of the "SYNC*" synchronization signal,
- one timer for the delaying of the "SYNC*" synchronization signal and
- one timer for program-run monitoring (watchdog), triggered by MMT4 every ms.

Two programmable 82C54 timers (timer 0 and timer 1) are used, with each timer containing three independently programmable, 16-bit decrementing counters.

Every counter has a control word register which must be programmed in line with the desired function.

Control word register

D 7							D 0
SC 1	SC 0	RL 1	RL 0	M 2	M 1	M 0	BCD

SCx = counter selection

RLx = selection as to how the counter value (setpoint) has to be loaded or as to how the counter contents have to be read. In the case of the processor board, setpoints are loaded only. The counter contents of 0 will be evaluated as an interrupt.

Binary values are loaded byte by byte, as follows:

RL1	RL0	Function
1	0	Loading the byte with the higher significance
0	1	Loading the byte with the lower significance
1	1	After the first command, loading the byte with the lower significance, and after the second command, loading the byte with the higher significance.

Mx = the counter are used as follows:

Timer 0 channel 0..2 in mode 2 (M2 = 0-Signal, M1 = 1-Signal, M0 = 0-Signal)
Timer 1 channel 0 in mode 3 (M2 = 0-Signal, M1 = 1-Signal, M0 = 1-Signal)
Timer 1 channel 1 in mode 5 (M2 = 1-Signal, M1 = 0-Signal, M0 = 1-Signal)
Timer 1 channel 2 in mode 1 (M2 = 0-Signal, M1 = 0-Signal, M0 = 1-Signal)

BCD = Selection of the binary or BCD code. In the case of the SPU 232, all counters work in the binary code (0-signal).

Counter selection

SC 1	SC 2	
0	0	Selection of counter 0 (channel 0)
0	1	Selection of counter 1 (channel 1)
1	0	Selection of counter 2 (channel 2)
1	1	not permitted

On the SPU 232, the counters are used as follows:

Timer 0

Channel	Type	Interrupt	Clock selection	Trigger selection	Triggering
Channel 0	MMT4	IRQ 1	TC 0	TT 0	TR 0
Channel 1	free timer	IRQ 16	TC 1	TT 1	TR 1
Channel 2	free timer	IRQ 3	TC 2	TT 2	TR 2

Timer 1

Channel	Type	Interrupt	Clock selection	Trigger selection	Triggering
Channel 0	SYNC* generation	IRQ 17	TC 3	TT 3	TR 3
Channel 1	SYNC* delay	IRQ 9	---	---	---
Channel 2	watchdog	IRQ 0	---	---	TR 4

Trigger and clock selection address 6000 H (I/O):

D 7							D 0
TT 3	TT 2	TT 1	TT 0	TC 3	TC 2	TC 1	TC 0

TTx = Trigger selection
0-signal = internal triggering (see "triggering")
1-signal = external triggering by VMEbus signal SYNC*

TCx = Clock selection
0-signal = internal frequency with f = 1 MHz
1-signal = externally with VMEbus signal SYNC*

Triggering address 6001 H (I/O):

D 7							D 0
X	X	X	TR 4	TR 3	TR 2	TR 1	TR 0

TRx = If internal triggering is selected (refer to "trigger and clock selection"), the pertinent timer is triggered by a "0" → "1" change of this bit.

Timer programming

Timer 0

Address 1003 H (I/O)	Command for control word register
Address 1000 H (I/O)	Binary value for channel 0
Address 1001 H (I/O)	Binary value for channel 1
Address 1002 H (I/O)	Binary value for channel 2

Timer 1

Address 2003 H (I/O)	Command for control word register
Address 2000 H (I/O)	Binary value for channel 0
Address 2001 H (I/O)	Binary value for channel 1
Address 2002 H (I/O)	Binary value for channel 2

2.4 Communication Interfaces

2.4.1 SPU 232 (Serial Interfaces)

The SPU 232 board has two serial interfaces for to connection to PCs. These interfaces permit an exchange of data at data rates of up to 38.4 kBd in the fully duplex mode. In order to reduce the load for the main processor, the serial interfaces are served by their own microcontroller (I/O processor). The I/O processor independently handles the serial data communication, including data checks (parity, framing, timeout conditions). The communication between main processor and I/O processor is routed via a 4-kByte dual-port RAM with a width of 16 bits. Complete commands (e.g. interface configuration) and/or records are always exchanged via this dual-port RAM.

Interface selection and data exchange take place under program control via the addresses FF04 0000 H ... FF04 0FFF H (determined by the MMT4 operating system).

Both serial interfaces are designed as potential-isolated RS-232C interfaces. They are non-isolated in relation to each other.

Connector layout of the serial interfaces (9-pin DSUB connectors)

Contact No.	Signal name	
1	free	
2	RxD	(receive data IN)
3	TxD	(send data OUT)
4	free	
5	GND	(0V)
6	free	
7	RTS	(send request OUT)
8	CTS	(ready to send IN)
9	free	

All the components for both serial interfaces (microcontrollers, optocouplers, D/C converters, RS-232C modules, etc.) are located on an additional board (piggy-back) which is fitted on the plug-type connectors of the SPU 232.

2.4.2 SPU 232-CAN (Serial and CANbus-Interface)

The SPU 232-CAN board has one serial interface (lower interface) for to connection to PCs. This interface permits an exchange of data at data rates of up to 38.4 kBd in the fully duplex mode. Additional the SPU 232-CAN board has one interface for connection to the CANbus (upper interface). In order to reduce the load for the main processor, the interfaces are served by their own microcontroller (I/O processor). The I/O processor independently handles the data communication, including data checks (parity, framing, timeout conditions). The communication between main processor and I/O processor is routed via a 4-kByte dual-port RAM with a width of 16 bits. Complete commands (e.g. interface configuration) and/or records are always exchanged via this dual-port RAM.

Both interfaces are designed as potential-isolated interfaces and they are also potential-isolated in relation to each other.

Connector layout of the serial interface (9-pin DSUB connectors)

Contact No.	Signal name	
1	free	
2	RxD	(receive data IN)
3	TxD	(send data OUT)
4	free	
5	GND	(0V)
6	free	
7	RTS	(send request OUT)
8	CTS	(ready to send IN)
9	free	

Connector layout of the CANbus interface (9-pin DSUB connectors)

Contact No.	Signal name	
1	free	
2	CAN_L	(CAN-LOW bus line)
3	CAN_GND	(0V)
4	free	
5	free	
6	CAN_GND	(0V)
7	CAN_H	(CAN-HIGH bus line)
8	free	
9	free	

All the components for both interfaces (microcontrollers, optocouplers, D/C converters, RS-232C and CANbus modules, etc.) are located on an additional board (piggy-back) which is fitted on the plug-type connectors of the SPU 232-CAN.

2.5 Local Bus Interface

The local bus interface with two plug-type connectors for coupling to expansion boards is not used on the SPU 232. The reserved address range for it is:

FF05 0000 H
⋮
FF05 FFFF H

2.6 Interface for an Additional Memory Card (Compact Flash)

The SPU 232 is fitted with a plug connector with a Compact Flash base, type 1, for operation of an additional Compact Flash-Card (≥ 4 MB). In the event that a Compact Flash-Card is needed and used, the operating system must be adapted accordingly.

Dialog addresses:

Control register FF06 8000 H
⋮
FF06 83FF H

Data register FF07 8000 H
⋮
FF07 83FF H

2.7 VMEbus Interface

For the purpose of data communication with other boards, the SPU 232 has an A32:D32 VME interface according to Revision C. The formats A32:D32, A32:D16, A32:D8, A24:D32, A24:D16, A24:D8, A16:D16 and A16:D8 are supported for active access to the VMEbus.

The SPU 232 has a read and write access to the VMEbus.

The VME address space and the associated address modifiers are selected under hardware control on the basis of the given physical addresses (mapping).

The following address areas are accessed:

A32 area: 0100 0000 H
⋮
FDFF FFFF H

The address areas 0000 0000 H ... 00FF FFFF H and FE00 0000 H ... FFFF FFFF H connot be addressed in the A32 address area.

A24 area: FE00 0000 H
⋮
FEFF FFFF H

A16 area: FFFE 0000 H
⋮
FFFE FFFF H

Note: The MMT 4 operating system works in accordance with the principle of paging, so that user programs do not have direct access to physical addresses. The "virtual" addresses for accesses to the VMEbus are obtained via operating-system calls.

The data bus width is selected as a function of the commands executed, such as:

```
mov   edx,  VMEADR   sets a VME address
mov   eax,  [edx]    performs a D32 access
mov   ax,   [edx]    performs a D16 access
mov   al,   [edx]    performs a D8 access
```

The VME interface also supports so-called unaligned transfers.

2.8 VMEbus Arbitration

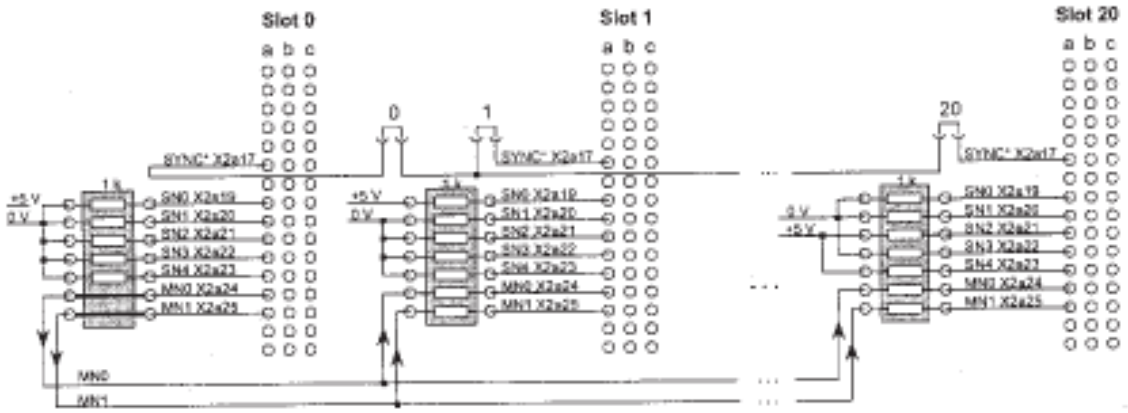
The SPU 232 comes with a Single-Level-VMEbus arbiter on the processor board. This arbiter cannot be deactivated. Only the bus request level 3 (BRQ3) is supported.

2.9 Basic Address in DPU.1, DPU-K or DPU-S subrack

In the DPU.1, DPU-K or DPU-S subrack, the slots on the J2 VMEbus board are subject to absolute location addressing from slot 0 to slot 20 (DPU.1), slot 11 (DPU-K) or slot 5 (DPU-S). Location addressing is performed via the "a"-row of the plug connectors of the J2 VMEbus board, whilst resistance networks (1kΩ switched to +5V and 0V) are used in order to adjust a binary-coded number of 0 ... 20 (DPU.1), 0 ... 11 (DPU-K) or 0 ... 5 (DPU-S) (*SN0 ... SN4*) for each location and the subrack (master or expansion subrack) is defined via another two connections (*MN0, MN1*).

The SPU 232 can only be installed in the master subrack (MN0 = 0, MN1 = 0) and there at slot 0. On the SPU 232 the connections X2a24 and X2a25 are connected to 0 V.

The J2 VMEbus board DPU.1 subrack features the following layout for the "a"-row with regard to SN0 ... SN4, MN0, MN1 and the SYNC* signal:



2.10 Base address for VMEbus subracks without location addressing

The location addressing system for the formation of the base address can be set on the SPU 232:

- by connector wiring when P2 connectors are available;
- internally on the SPU 232 by means of the DIP switch S1.

Slot address 0 must be set for the SPU 232 as a precondition for the start-up of the MMT4 operating system.

In the case of the connector wiring option, a binary-coded number of 0 ... 20 (slots 0 ... 20) is wired via the X2a19 ... X2a23 connections, whereby the 1-signal is generated by a connection to +5 V and the 0-signal by a connection to 0V (GND) ($SN0 = 2^0$, $SN1 = 2^1$, $SN2 = 2^2$, $SN3 = 2^3$, $SN4 = 2^4$).

Adjustment by means of the DIP switch S1 is necessary if the SPU 232 is used in a subrack without an J2 VMEbus board.

Setting the location address:

S1 - 1	^	2^0
S1 - 2	^	2^1
S1 - 3	^	2^2
S1 - 4	^	2^3
S1 - 5	^	2^4
S1 - 6	^	MN0 (position "ON") *"Master subrack"*
S1 - 7	^	MN1 (position "ON") *"Master subrack"*
S1 - 8	^	without function.
Position "ON"	^	0-signal
"OFF"	^	1-signal

2.11 Reset Control

When the supply voltage is connected or when a switching pin is inserted into socket 131 (Main Reset), apart from the local reset, initialization and program start, a temporary SYSRESET* is passed on to the VMEbus (connection X1c12).

2.12 Interrupt Processing

The SPU 232 processes the following internal interrupt requests:

Interrupt request IRQ0	:	Timer 1, channel 2 (watchdog)
Interrupt request IRQ1	:	Timer 0, channel 0 (MMT4)
Interrupt request IRQ2	:	Serial interface (pos. 58) of the reception channel
Interrupt request IRQ3	:	Timer 0, channel 2 (free timer)
Interrupt request IRQ4	:	No function
Interrupt request IRQ5	:	No function (local bus interface to expansion board)
Interrupt request IRQ6	:	No function (local bus interface to expansion board)
Interrupt request IRQ7	:	No function (local bus interface to expansion board)
Interrupt request IRQ8	:	
Interrupt request IRQ9	:	Timer 1, channel 1 (SYNC* delay)
Interrupt request IRQ10	:	Request from flash disk
Interrupt request IRQ11	:	Serial interface (pos. 72) of the reception channel
Interrupt request IRQ12	:	No function (local bus interface to expansion board)
⋮		
Interrupt request IRQ15	:	
Interrupt request IRQ16	:	Timer 0, channel 1 (free timer)
Interrupt request IRQ17	:	Timer 1, channel 0 (SYNC* generation)
Interrupt request IRQ18	:	VMEbus interrupt 1
Interrupt request IRQ19	:	VMEbus interrupt 2
Interrupt request IRQ20	:	VMEbus interrupt 3
Interrupt request IRQ21	:	VMEbus interrupt 4
Interrupt request IRQ22	:	VMEbus interrupt 5
Interrupt request IRQ23	:	VMEbus interrupt 6
Interrupt request IRQ24	:	VMEbus interrupt 7 (highest priority)

2.13 EMC Register

The EMC sensor on the board measures the electromagnetic alternating field to which the board is exposed. Level 1 (EMC 0) is activated in the case of the interference level III standardized according to IEC 801-4. At this level, the board is still working in a reliable manner under laboratory conditions. This message, however, must already be interpreted as a warning.

Level 2 (EMC 1) is activated in the case of the interference level IV standardized according to IEC 801-4. The proper operation of the board is no longer ensured at this level. This message must be interpreted as a fault message.

The messages are stored in status register 2 (D5 = EMC 0, D6 = EMC 1) which can be read with the address 4000 H. The EMC messages are reset during writing into this register.

3 Using the SPU 232 under Logidyn D2

The SPU 232 can be used both for Logidyn D2 applications and for standard-language programs. The MMT4 (**M**icro **M**ulti **T**asking Version 4) operating system was developed for this purpose. This operating system enables multi-tasking operation on an SPU 232. Under MMT4, up to 32 tasks at up to 32 different priority levels can be executed on the SPU 232. The operating system itself requires 5 tasks for monitoring and controlling (RDT4 = **R**ealtime **D**ebugging **T**ool Version 4) and/or for communication via the V.24 interface(s). All the tasks are performed as real 32-bit applications in protected memory areas (protected mode), so that mutual interference is avoided. All the user tasks can be reloaded, stopped and re-started online.

Logidyn D2 applications require a management task and the tasks which process the programs developed under LogiCAD. These program tasks exist in duplicate in order to ensure quick switching over for online programming.

In the flash memory described in *section 2.2* , a file system is implemented where the entire system and application software is stored. A suitable application (WinRDTM) exists for the communication with the MMT4 for the engineering PCs under Windows 3.x or Windows NT. This WinRDTM application is used for loading the files into the target machine and for manipulating and debugging the tasks.

Whereas the connection to the serial interfaces are integrated in the MMT4 operating system, it is neccessary to load a driver task if using the CANbus interface of the SPU 232-CAN.

Basic initialization and firmware installation of the SPU 232

In the as-delivered condition of the SPU 232, the status of the flash memory is not defined, i.e. it contains neither the system nor the application software. This means that the flash memory first of all must be formatted. This is done by loading the MEDIUM.xxx file which is available in the \LOGIDYN2\HLL directory using tab control "Online" of the hardwareconfiguration of LogiCAD. Thereafter, the created configuration file of the Logidyn D2 configuration is loaded into the SPU 232.

When the SPU 232 is used for the first time, or after it has been replaced, a pin should be inserted into switching socket 319 prior to connecting the supply voltage in order to prevent unintended starting of the configuration. This is important in cases in which a configuration file of a configuration is already stored on the SPU 232.

4 Connector Layout

- **VMEbus connector layout P1 (position X1)**

Contact No.	Signal names Row a	Row b	Row c
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5*
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12 V	+ 5 V STDBY	+12 V
32	+ 5 V	+ 5 V	+ 5 V

96-pin multipoint connector P1 (top)

□ SPU 232 connector layout

GND 0 V, Reference point for +5 V (UB5)

- **VMEbus connector layout P2 (position X2)**

Contact No.	Signal names Row a	Row b	Row c
1		+5 V	
2		GND	
3			
4		A 24	
5	POWFAIL *	A 25	
6		A 26	
7		A 27	
8		A 28	
9		A 29	
10		A 30	
11		A 31	
12		GND	
13		+5 V	
14		D 16	
15		D 17	
16		D 18	
17	SYNC*	D 19	
18		D 20	
19	SN0 1)	D 21	
20	SN1 1)	D 22	
21	SN2 1)	D 23	
22	SN3 1)	GND	
23	SN4 1)	D 24	
24	MN0 1)	D 25	
25	MN1 1)	D 26	
26		D 27	
27		D 28	
28		D 29	
29		D 30	
30		D 31	
31		GND	
32		+5 V	
96-pin multipoint connector P2 (bottom)			

☐	SPU 232 connector layout
SYNC *	Synchronization signal for DPU. It is activated by installing the on VMEbus board J2.
SN0 ... SN4	Location addressing
MN0, MN1	Selection of "master or expansion subrack 1 to 3 ". SPU 232 in the master subrack only!
GND	0 V (M5), reference point of +5 V (UB5)
1)	Signals are not continuously on the J2-VMEbus board. They are, only connected to the connections.

DSUB-connector (9-pin) on the front panel Pos. 58, 72 for SPU 232 and Pos. 72 for SPU 232-CAN

Contact No.	Signal name	
1	free	
2	RxD	(receive data IN)
3	TxD	(send data OUT)
4	free	
5	GND	(0V)
6	free	
7	RTS	(send request OUT)
8	CTS	(ready to send IN)
9	free	

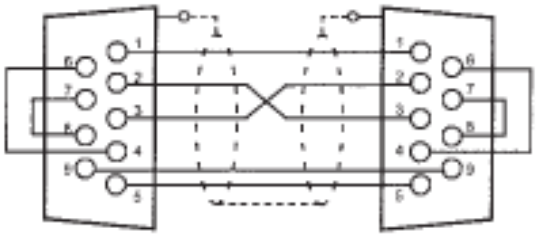
Interface: RS-232C

DSUB-connector (9-pin) on the front panel Pos. 58 for SPU 232-CAN

Contact No.	Signal name	
1	free	
2	CAN_L	(CAN-LOW bus line)
3	CAN_GND	(0V)
4	free	
5	free	
6	CAN_GND	(0V)
7	CAN_H	(CAN-HIGH bus line)
8	free	
9	free	

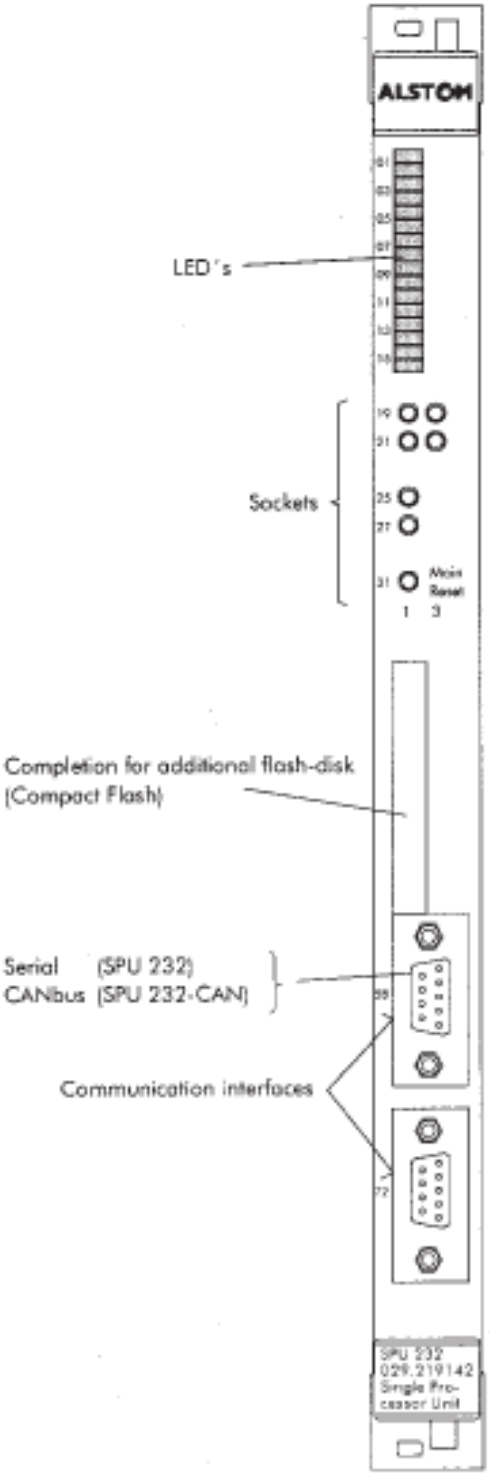
Connection cable PC-V24:

Adapter cable (Article No.: 029.134499)



(9-pin DSUB socket) (9-pin DSUB socket)

5 Front Panel



5.1 Front Panel Elements

The coordinates are read as follows:

Numbers from the left

1st digit	=	column
2nd and 3rd digit	=	line

Additionally for the vertically arranged LEDs

Coordinate marked "A"	=	upper LED
Coordinate marked "B"	=	lower LED

- **Switching sockets**

119	Suppresses the memory test during booting
319	Start disable for the operating system
121	Start disable for the application software
321, 125, 127	Currently not used
131	**Main Reset:** local Reset on SPU 232 and SYSRESET* output to VMEbus. (SPU 232 is arbiter at VMEbus !)

- **LEDs**

101A **red LED:** "Program monitoring" (watchdog)

This LED represents the result of three tests, i.e.:

1) self-test:
Following a RESET or connection of the supply voltage, the SPU 232 performs a self-test in order to check the individual functional parts of the board.
The LED flashes during the self-test. If the LED still flashes after some seconds, this indicates a fault of the board.
If the result remains negative despite several RESET attempts, the SPU 232 must be replaced.

2) bootstrap procedure:
On successful completion of the SPU 232 self-test, the bootstrap procedure is automatically started in order to load the programs (operating system, Logidyn D2 and user program) from the flash-disk into the main memory. During this phase, the LED is lit (steady light). If the LED still lit after 30 seconds, this indicates that the bootstrap procedure has failed.
If the board fails to properly perform the bootstrap procedure despite several RESET attempts, the SPU 232 must be replaced.

3) program monitoring:
The LED is dark on successful completion of the bootstrap procedure and proper execution of the operating system MMT4.
If the LED is lit, this may indicate a fault of the board.
If the proper function of the board is not achieved despite several RESET attempts, the SPU 232 must be replaced.

101B **red LED:** "RESET"

The LED is lit in the case of a RESET (switching pin in socket 131).

The meanings of the LEDs 103, 106 and 109 are not defined while this LED is lit.

103A **red LED:** "Battery monitoring"

The LED indicates the battery status of the "+5 VSTDBY" battery voltage supplied via the VMEbus.

If the LED is lit, this indicates that the battery voltage is either too low or is not available. If no battery voltage is available, the lithium battery on the processor board saves the data stored for approx. 4 years at 25 °C.

Note: Operating system, Logidyn D2, and the user programs are stored on the flash-disk in a non-volatile manner. The battery-buffered memory holds only the Logidyn D2 variables.

103B **red LED:** "Fault/error"

Depending on possible faults or errors of the firmware, the LED either flashes or is permanently lit.

LED flashes at a frequency of f = 4 Hz:
The LED flashes at this frequency if one or more tasks in the MMT4 "get stuck" (in order to find the possible cause, use WinRDTM or MMT4-Debug).

LED flashes at a lower frequency:
Logidyn D2 Runtime does not find any valid files, i.e. invalid version No. (in order to find the possible cause, use WinRDTM or MMT4-Debug).

LED is permanently lit:
Initialization of the Communication Manager has failed, or invalid data on the flash-disk.

105A **red LED:** "Bus error"

The LED is lit in the case of access to a VMEbus station which fails to reply within the time ($t < 32\ \mu s$) defined for this purpose.

105B **yellow LED:** " processor board ready"

The yellow LED is lit as long as the internal initialization of the hardware is not complete. The processor board outputs the SYSFAIL* signal as long as the LED is lit. If the LED is still lit after the supply voltage has been disconnected and reconnected again, the SPU 232 must be replaced.

107A **yellow LED:** "Warning"

The LED flashes at a frequency of f = 2 Hz if one or more desired Logidyn D2 programs exceed the polling time.

Possible remedies are reducing the number of modules or increasing the polling time.

The LED continues flashing another 2 seconds after the overload condition has been eliminated.

107B **green LED:** "RUN"

The LED displays the status of the communication. The LED flashes while a data dialog is underway.

109A **green LED:** "SYSCON"

The LED is always lit, because the SPU 232 is arbiter.

109B **green LED:** "User 1"

This LED is lit, if Logidyn D2 is running.

111A **green LED**

This LED has no function.

111B **green LED:** "Serial"

The LED is lit if the serial interface sends an interrupt to the SPU 232.

113A **green LED**

This LED has no function.

113B **green LED:** "VME access"

The LED is lit while the SPU 232 accesses another VMEbus station.

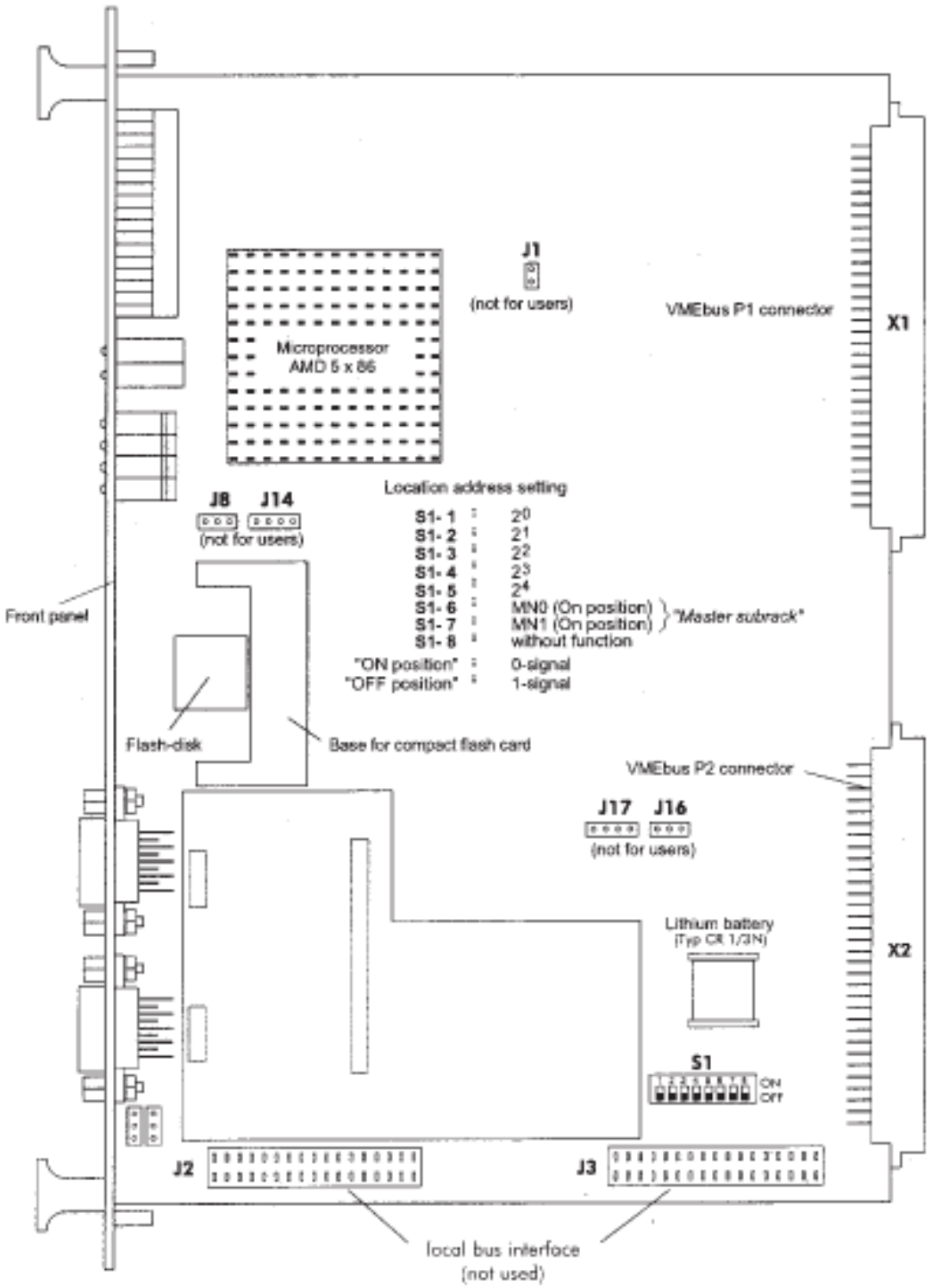
115A **green LED:** "SYNC-OK"

The LED is lit if the SYNC* clock is available on the VMEbus board J2 of the DPU.1, DPU-K or DPU-S subrack. The SYNC* clock must be generated either by the DHC 100 communication board or by the SPU 232 itself.

115B **green LED**

This LED has no function.

6 Assembly Diagram



7 Technical Specifications

Power Supply

- **VMEbus processing**

UB5	=	+5 V, ±3 %
M5	=	Reference point (GND) of UB5
Ityp	=	2 A

Serial Interfaces

- **Communication interfaces, Pos. 58 and 72 for SPU 232**

Interfaces	RS-232C

- **Communication interfaces, Pos. 58 and 72 for SPU 232-CAN**

Interface Pos. 58	CANbus
Interface Pos. 72	RS-232C

Ambient Conditions

Ambient temperature	0° to + 55° C (with forced air circulation of 0.5 m/s)
Storage temperature	-40° C to +85° C
Humidity	Class F

Electromagnetic Compatibility (in the DPU subrack)

- Standard (pr) EN 50081-2 for noise emission
- Standard (pr) EN 50082-2 for noise immunity

Mechanical Design

- INTERMAS format

Size	6 - 04
Dimensions	approx. 233.4 mm x 160 mm x 20.5 mm (h x d x w)

- Connectors

VMEbus P1	E96M-C1A, connections X1
VMEbus P2	E96M-C1A, connections X2
Weight	approx. 400 g

Reorder Data

Type	SPU 232
Article No.	029.219142
Type	SPU 232-CAN
Article No.	029.219153

Bernhard WALTER
22.04.2005 17:34

An: jutta.lehrmann@powerconv.alstom.com
cc: Jacqueline LAQUA-KOEHLER/DEDRS01/TDE/AREVA-TD@ATD, Uwe KALTENBORN/DEDRS01/TDE/AREVA-TD@ATD, Hermann DICKS/DEDRS01/TDE/AREVA-TD@ATD, Erik STANDHARDINGER/DEDRS01/TDE/AREVA-TD@ATD

Thema: Ihre Re Nr. 1800042961 vom 25.2.05

Sehr geehrte Frau Lehrmann,

Die genannte Rechnung können wir in ihrer pauschalen Form nicht akzeptieren, da sie sich auf unterschiedliche Vorgänge bezieht. Bitte trennen Sie die gezeigten Personalleistungen vom Mietpart ab.

Die Personalleistungen werden wir vorbehaltlich einer noch zu treffenden Einigung über die Abwicklung der Thyrow-Probleme im Bereich der VDM7000-Umrichter erst einmal bezahlen.
Die zweite Forderung über Miete der Hochspannungslastteiler in Höhe von 6840 EURO bitten wir zu überdenken und zurückzuziehen oder zumindest bis zum Abschluß der gemeinsamen Fehlersuche zurückzustellen. Andernfalls würden wir uns dann gezwungen sehen, ebenfalls eine Mietrechnung zu stellen und zwar über die Nutzung von Umrichtermodulen aus unseren Beständen der Anlagen 7 und 8.

Bitte sprechen Sie in dieser Angelegenheit Herrn Dr. Möhlenkamp und auf unserer Seite Herrn Dicks an.

Mit freundlichen Grüßen,

AREVA T&D, Berlin
PEB

Bernhard Walter

ALSTOM

DEP 232.1
Input Board

Article No. 029.223003

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Scope of validity:

ALSTOM
Power Conversion GmbH

Revision state

Rev.	Pages concerned	Remarks	Date	Designed Dept. / Name	Reviewed Dept. / Name	Approved Dept. / Name
00	all	new	06/00	E45 Hr. Hampf	E45 Hr. Behrendt	E4 Dr. Groschupf

CONTENTS

1 General

The input board DEP 232.1 has 32 potential-free inputs. The front panel is provided with LEDs for the indication of input signal status information, as well as sockets for the simulation (1-signal) of the inputs by means of switching pins.

The DEP 232.1 is a VMEbus plug-in board of double Euroformat size (6 height units [HEs]) and with a width of 4 TE (depth units).

Note: The DEP 232.1 board is the downward-compatible successor board to the DEP 232 board (article No. 590.043152). The following additional functions, which are not supported in Logidyn D2, were implemented: switchable operation time class for all inputs and generation of vectored interrupts.

2 Functional Description

The board contains 32 potential-free inputs the reference points of which are combined in 6 groups. All groups are potential-isolated against each other and against the processing level (5V, VMEbus).

Group definition:

Input connections	Associated reference point
inputs 1 ... 8 (group 1), X4a2 ... X4a16	MS1, (X4c32)
inputs 9 ... 16 (group 2) X4a18 ... X4a32	MS2, (X4c28)
inputs 17 ... 24 (group 3) X4e2 ... X4e16	MS3, (X4c24)
inputs 25 ... 27 (group 4) X4e18 ... X4e32	MS4, (X4c20)
inputs 30 (group 5) X4e24 ... X4e28	MS5, (X4c16)
inputs 31 ... 32 (group 6) X4e30 ... X4e32	MS6, (X4c8)

The periphery (inputs and reference points MS1 ... MS6) is connected via the 48-pin plug connector **X4** on the front panel.

The board is compatible with the DEP 085.2 in terms of input connections and associated reference points.

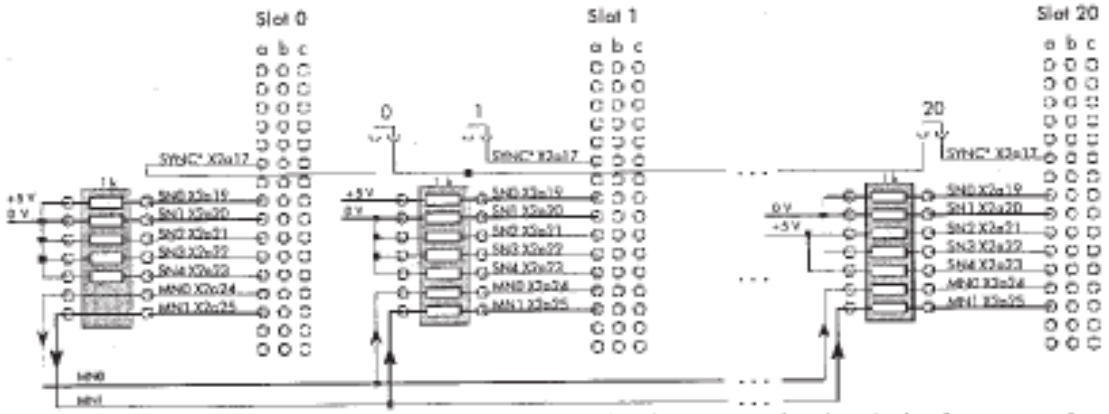
2.1 Addressing

The board has a VMEbus slave interface. It uses a 1-kByte address space in the A24:D16 address area. It is designed for use in the DPU, DPU-K or DPU-S subrack, but it may also be used in the standard VMEbus subrack.

2.1.1 Base Address in DPU, DPU-K or DPU-S subrack

In the DPU, DPU-K or DPU-S subrack, the slots on the J2 VMEbus board are subject to absolute location addressing from slot 0 to slot 20 (DPU), slot 11 (DPU-K) or slot 5 (DPU-S). Location addressing is performed via the "a"-row of the plug connectors of the J2 VMEbus board, whilst resistance networks (1kΩ switched to +5V and 0V) are used in order to adjust a binary-coded number of 0 ... 20 (DPU), 0 ... 11 (DPU-K) or 0 ... 5 (DPU-S) (*SN0 ... SN4*) for each location and the subrack (master or expansion subrack) is defined via another two connections (*MN0, MN1*).

The J2-VMEbus board in the DPU features the following configuration for the "a"-row with regard to SN0 ... SN4, MN0, MN1 and the "SYNC*" signal:



With this layout, the DEP 232.1 can be used and addressed in the master subrack or in the three expansion subracks.

The DEP 232.1 generates the following basic addresses on the basis of the slot (location) addresses:

Slot	Master		Expansion board 1		Expansion board 2		Expansion board 3	
	Board address	Internal basic address	Board address	Internal basic address	Board address	Internal basic address	Board address	Internal basic address
0	0	E40000 H	21	E48000 H	42	E50000 H	63	E58000 H
1	1	E40400 H	22	E48400 H	43	E50400 H	64	E58400 H
2	2	E40800 H	23	E48800 H	44	E50800 H	65	E58800 H
3	3	E40C00 H	24	E48C00 H	45	E50C00 H	66	E58C00 H
4	4	E41000 H	25	E49000 H	46	E51000 H	67	E59000 H
5	5	E41400 H	26	E49400 H	47	E51400 H	68	E59400 H
6	6	E41800 H	27	E49800 H	48	E51800 H	69	E59800 H
7	7	E41C00 H	28	E49C00 H	49	E51C00 H	70	E59C00 H
8	8	E42000 H	29	E4A000 H	50	E52000 H	71	E5A000 H
9	9	E42400 H	30	E4A400 H	51	E52400 H	72	E5A400 H
10	10	E42800 H	31	E4A800 H	52	E52800 H	73	E5A800 H
11	11	E42C00 H	32	E4AC00 H	53	E52C00 H	74	E5AC00 H
12	12	E43000 H	33	E4B000 H	54	E53000 H	75	E5B000 H
13	13	E43400 H	34	E4B400 H	55	E53400 H	76	E5B400 H
14	14	E43800 H	35	E4B800 H	56	E53800 H	77	E5B800 H
15	15	E43C00 H	36	E4BC00 H	57	E53C00 H	78	E5BC00 H
16	16	E44000 H	37	E4C000 H	58	E54000 H	79	E5C000 H
17	17	E44400 H	38	E4C400 H	59	E54400 H	80	E5C400 H
18	18	E44800 H	39	E4C800 H	60	E54800 H	81	E5C800 H
19	19	E44C00 H	40	E4CC00 H	61	E54C00 H	82	E5CC00 H
20	20	E45000 H	41	E4D000 H	62	E55000 H	83	E5D000 H
	$\overline{MN0}$ & $\overline{MN1}$		MN0 & $\overline{MN1}$		$\overline{MN0}$ & MN1		MN0 & MN1	

Subrack selection:

$\overline{MN0}$ or $\overline{MN1}$ ≙ 0-signal
MN0 or MN1 ≙ 1-signal

Slot 0:

This slot is only for the VCM 232.1, SPU 232 and MCU 232 (master subrack) or VCS 232 (expansion subrack).

2.1.2 Basic Address for VMEbus Subrack without DPU

The slot (location) address for the generation of the basic address can be adjusted on the DEP 232.1:

- by suitable plug connector wiring if P2 plug connectors are available;
- internally on the DEP 232.1 by means of DIP switch S1.

In the case of the plug connector wiring, a binary coded number of 0 ... 20 (Slot 0 ... 20) is wired via the connectors X2a19 ... X2a23. The 1-signal is generated by connection to +5V, whilst the 0-signal is generated by connection to 0V (GND) (SN0 = 2^0, SN1 = 2^1, SN2 = 2^2, SN3 = 2^3, SN4 = 2^4). The same applies to the rack selection MN0/MN1.

Adjustment by means of DIP switch S1 is necessary if the DEP 232.1 is used in a subrack without a P2 plug connector.

Adjusting the slot (location) address:

S1 - 1		⌢	2^0
S1 - 2		⌢	2^1
S1 - 3		⌢	2^2
S1 - 4		⌢	2^3
S1 - 5		⌢	2^4
Position	„ON"	⌢	0-signal
	„OFF"	⌢	1-signal

2.2 Address Modifier

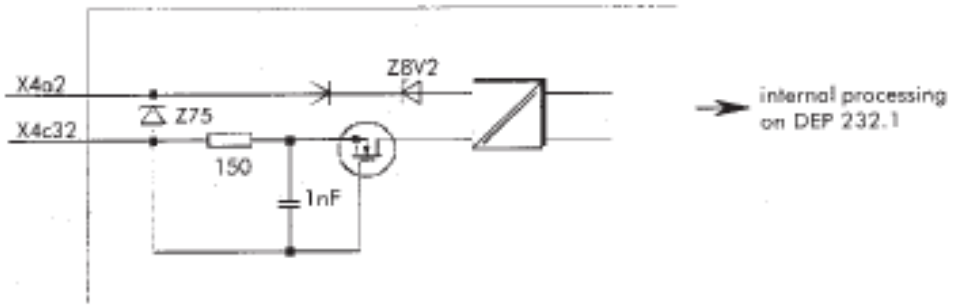
The DEP 232.1 only responds to user and supervisor data accesses with AM codes (AM0 ... AM5) for the A24:D16 area (standard). 39H or 3DH can be preset as AM codes.

BERR* is output in the event of an access to the DEP 232.1 in A24:D16 with LWORD* active. This also applies to an attempt to write into the identification register.

2.3 Inputs

The 32 inputs have the following structure:

example: **Input** 1



All inputs feature a switch-on (make) threshold, constant-current behavior and a Zener diode with U = 75 V in order to limit input voltage peaks.

The inputs X4a2 ... X4a32 and X4e2 ... X4e22 have an input signal delay which can be determined via the data dialog register *(see para. 3.4)* common to t = 4 ms (operation time class IV)) or t = 0.5 ms (operation time class II). In the case of the inputs X4e24 ... X4e32, the switch-on (make) delay of t = 4 ms (operation time class IV) or t = 0.5 ms (operation time class II) can be determined for each input via the data dialog registe*).*

2.3.1 Display and Simulation of Input Signals

The front panel provides, for all inputs, LEDs and simulation possibilities for the input signals. Active process signals (1-signal) or simulated process signals are indicated by a green LED which is then lit.

The input signals (1-signal only) are simulated by inserting switching pins into the sockets allocated to the inputs, however, subject to the condition that the simulation function has been enabled.

This is achieved for all inputs together by inserting a switching pin into the "FREI-SIM" (ENABLE SIM) socket and by the setting of the simulation enable flag in the command register *(see para. 3.1)*. The input signals cannot be simulated if the bit is deleted (reset) in the command register.

The red "FREI-SIM" (ENABLE SIM) LED signals the enabled condition of the simulation function. The LED goes on briefly when the supply voltage is connected.

2.4 Function Control of the DEP 232.1

The following functions can be determined via the command register *(see para. 3.1)*:

- Start bit

  Only during the initialization phase, the board is not ready for operation after a SYSRESET* or after the connection of the supply voltage (UB5). Thereafter, the board is capable of reading input signals (periphery or simulated input signals).

  The start bit can be used in order to directly check whether the DEP 232.1 can be addressed by the central unit.

- Asynchronous or Synchronous Mode

  The DEP 232.1 can work in the asynchronous and synchronous mode.

  In the case of the asynchronous mode, the values read in always corresponds to the process signals which are available externally (with the exception of the delay of the signals in accordance with the operation time classes). In the case of the synchronous mode, the process signals are always polled with the falling edge of the SYNC* signal (X2a17) only and then remain stable until the next SYNC*.

  The switching over between the modes is performed by the software via the command register. In the event that the synchronous mode has been selected, and if the synchronization signal SYNC* fails to arrive within $t \leq 10$ ms, the board automatically changes to the asynchronous mode.

2.5 EMC Register

The EMC sensor on the board measures the electromagnetic, alternating field to which the board is exposed.

Level 1 responds in the event of a standard fault level III according to IEC 801-4, where the reliable operation of the board is still ensured under laboratory conditions. However, this message must already be regarded as a warning.

Level 2 responds in the event of a standard fault level IV according to IEC 801-4, where the reliable operation of the board is no longer ensured. This message must be regarded as a fault signal.

Bit 6 and bit 7 of the status register *(see para. 3.3)* indicate the degree of EMC exposure.

2.6 Vectorized VMEbus interrupts

The DEP 232.1 board is capable of generating vectorized interrupts at the VMEbus. The X4e18...X4e32 inputs can be selected as the signal sources. The interrupt function can be separately activated for every input. Every input can be programmed for an interrupt with a rising or falling edge. The interrupt vector is modified depending on the interrupt source. The base value of the interrupt vector can also be set via the software. This function permits the activation of a special interrupt service routine via every input, so that program processing becomes particularly effective.

Interrupt processing proceeds on the basis of the following system:

A base value of **xxxyyyzzB** (binary) is loaded into register for the interrupt vector base value *(refer to section 3.5)*. The value of **yyy** represents the interrupt levels IRQ1..7 (binary coded). A value of 0 is permissible and disables all interrupt functions.

This base value is then modified as a function of the interrupt source. The values of **xxx** and **zz** of the base value remain unchanged. The following interrupt vector is then output from the signal source (independent of the contents of yyy):

Resultant interrupt vector for signal source e18:	xxx000zzB
Resultant interrupt vector for signal source e20:	xxx001zzB
Resultant interrupt vector for signal source e22:	xxx010zzB
Resultant interrupt vector for signal source e24:	xxx011zzB
Resultant interrupt vector for signal source e26:	xxx100zzB
Resultant interrupt vector for signal source e28:	xxx101zzB
Resultant interrupt vector for signal source e30:	xxx110zzB
Resultant interrupt vector for signal source e32:	xxx111zzB

Due to the position of the vector modification within the vector byte, modification is effectively carried out in steps of four.

If several interrupt sources are active at the same time, the interrupt vector is generated on the basis of the source with the highest priority. Signal source e32 has the highest, e18 the lowest priority.

During the interrupt acknowledge cycle, the internal interrupt request registers are frozen, so that metastable states are avoided. The interrupt request memory of the processed input is automatically reset (ROA option) during an interrupt acknowledge.

Example: If a value of 101**110**00B is set as the interrupt base value, and if the interrupt comes from signal source input e22, the interrupt is triggered at **IRQ6** , with the resultant vector being 101010**0**0B = 0A8H.

3 Dialog Registers

The dialog with the VMEbus is handled via these registers, as follows:

Basic address	Access	Data size	Remarks
+ 0 H	read/write	2 bytes	Command register, *see para. 3.1*
+ 2 H	read only	2 bytes	Acknowledgement register, *see para. 3.2*
+ 4 H	read only	2 bytes	Status register, *see para. 3.3*
+ 6 H	read only	2 bytes	Fault code register (0x0)
+ 8 H	read only	8 char	Identification, basic board type **DEP 232**
+ 10 H	read only	8 char	Identification, board type **DEP 232.1**
+ 18 H	read only	4 char	Identification, manufacturer **eac**
+ 1C H	read only	10 char	Identification, article No.: 029.223003
+ 26 H	read only	2 char	Identification, revision code (0x0)
+ 28 H	read only	4 char	Identification, date of manufacture, e.g. 0595 (05th week 95)
+ 2C H	read only	8 char	Identification, serial No. (xxxxxxxx)
+ 34 H	read only	8 char	Identification, firmware version (0x0)
+ 3C H	read only	2 bytes	Identification, assembly variant (0x0020)
+ 3E H	read only	2 bytes	Identification, free description (0x0)
+ 80 H	read/write	2 Byte	Input signal delay 4 ms/0,5 ms für e2..e22
.....			(this value appears in all addresses + 80 H..+ B4 H)
+ B4 H	read/write	2 Byte	Input signal delay 4 ms/0,5 ms für e2..e22
+ B6 H	read/write	2 Byte	Input signal delay 4 ms/0,5 ms für e24
+ B8 H	read/write	2 Byte	Input signal delay 4 ms/0,5 ms für e26
+ BA H	read/write	2 bytes	Input signal delay 4 ms/0.5 ms for e28
+ BC H	read/write	2 bytes	Input signal delay 4 ms/0,5 ms for e30
+ BE H	read/write	2 bytes	Input signal delay 4 ms/0.5 ms for e32
+ C0 H	read/write	2 Byte	Interrupt vector base value
+ F0 H	read/write	2 Byte	Interrupt enable register input e18
+ F2 H	read/write	2 Byte	Interrupt enable register input e20
+ F4 H	read/write	2 Byte	Interrupt enable register input e22
+ F6 H	read/write	2 Byte	Interrupt enable register input e24
+ F8 H	read/write	2 Byte	Interrupt enable register input e26
+ FA H	read/write	2 Byte	Interrupt enable register input e28
+ FC H	read/write	2 Byte	Interrupt enable register input e30
+ FE H	read/write	2 Byte	Interrupt enable register input e32
+ 100 H	read only	2 bytes	Take-over of input signal states from a2 ... a32
+ 102 H	read only	2 bytes	Take-over of input signal states from e2 ... e32
+ 104 H	read only	2 bytes	mirroring of <basic address + 100 Hb>
+ 106 H	read only	2 bytes	mirroring of <basic address + 102 Hb>

3.1 Command Register

The following functions are implemented in the command register:

Bit No.	Description	Action	Remarks
0			0
1			0
2			0
3			0
4	Fault message	static	Reset bit 6 and bit 7 in the status register
5	Start bit	Edge 0 → 1	Set bit 5 in the acknowledge register.
6			0
7			0
8	Mode of operation	static	1 = asynchronous 0 = synchronous
9	Simulation	static	1 = enabled 0 = disabled
10			0
11			0
12			0
13			0
14			0
15			0

Explanations:

Bit 4 : Reset of the fault memory by the software.

Bit 5 : See "startbit" *(para. 2.4)*.

Bit 8 : See "asynchronous or synchronous mode" *(para. 2.4)*.

Bit 9 : See " display and simulation of input signals " *(para. 2.3.1)*.

Bits 0 to 8 and 10 to 15 are reset (0 signal), and bit 9 is set to 1-signal by a SYSRESET* or by the connecting of the supply voltage (UB5).

3.2 Acknowledgement Register

The following bits of the command register are acknowledged in the acknowledgement register of the DEP 232.1:

Bit No.	Description	Remarks	
0		0	
1		0	
2		0	
3		0	
4	Fault message	1 = acknowledgement performed *(see para 3.1)*	
5	Start bit	1 = after the presetting of the start bit	0 = after a SYSRESET or after a power-on
6		0	
7		0	
8	Mode of operation	1 = asynchronous	0 = synchronous
9	Simulation	1 = simulation enabled	0 = simulation disabled
10		0	
11		0	
12		0	
13		0	
14		0	
15		0	

3.3 Status Register

The following messages are available in the status register of the DEP 232.1:

Bit No.	Description	Remarks	
0	Initialization	1 = Initialization underway	0 = board completely initialized
1		0	
2		0	
3		0	
4		0	
5		0	
6	Warning EMC sensor	1 = EMC level 1 exceeded	0 = ok.
7	Warning EMC sensor	1 = EMV level 2 exceeded	0 = ok.
8	Synchro clock SYNC* (P2 plug connector)	1 = Synchro clock t > 10 ms	0 = synchro clock t $\leq$ 10 ms
9	Simulation	1 = Simulation active	0 = Simulation disabled
10		0	
11	VME access [1]	1 = VME access t > 130 ms (Time out)	0 = accesses t < 130 ms
12		0	
13		0	
14		0	
15		0	

1) only valid for read accesses to the data dialog register (input register).

3.4 Data Dialog Register

(Special register for interrupt functions see para. 3.5)

Basic-address	Description	Access	Size	Remarks
+ 80 H	Input delay	read/write	2 Byte	Signal delay for input a2..e22 Bit D8: 1 = 0,5 ms (Op.-class II) 0 = 4 ms (Op.-class IV)
.....	Input delay	read/write	2 Byte	Signal delay for input a2..e22 Bit D8: 1 = 0,5 ms (Op.-class II) 0 = 4 ms (Op.-class IV)
+ B4 H	Input delay	read/write	2 Byte	Signal delay for input a2..e22 Bit D8: 1 = 0,5 ms (Op.-class II) 0 = 4 ms (Op.-class IV)
+ B6 H	Input delay	read/write	2 bytes	Signal delay for input e24 Bit D8: 1 = 0.5 ms (Op. class II) 0 = 4 ms (Op. class IV)
+ B8 H	Input delay	read/write	2 bytes	Signal delay for input e26 Bit D8: 1 = 0.5 ms (Op. class II) 0 = 4 ms (Op. class IV)
+ BA H	Input delay	read/write	2 bytes	Signal delay for input e28 Bit D8: 1 = 0.5 ms (Op. class II) 0 = 4 ms (Op. class IV)
+ BC H	Input delay	read/write	2 bytes	Signal delay for input e30 Bit D8: 1 = 0.5 ms (Op. class II) 0 = 4 ms (Op. class IV)
+ BE H	Input delay	read/write	2 bytes	Signal delay for input e32 Bit D8: 1 = 0.5 ms (Op. class II) 0 = 4 ms (Op. class IV)
+ C0 H	Interrupt vector base value	read/write	2 byte	see para. 3.5
+ F0 H	Interrupt enable register	read/write	2 byte	see para. 3.5
.....	Interrupt enable register	read/write	2 byte	see para. 3.5
+ FE H	Interrupt enable register	read/write	2 byte	see para. 3.5
+ 100 H	Binary inputs, "a"-row	read only	2 bytes	Take-over of input states from a2 .... a32
+ 102 H	Binary inputs, "e"-row	read only	2 bytes	Take-over of input states from e2 .... e32
+ 104 H	Binary inputs, "a"-row	read only	2 bytes	Mirror image of basic address + 100 H>
+ 106 H	Binary inputs, "e"-row	read only	2 bytes	Mirror image of basic address + 102 H>

3.5 Special Register for Interrupt Functions

Basic-address	Description	Access	Size	Remarks
+ C0 H	Interrupt vector base value	read/write	2 bytes	Bit 0 ... Bit 7: without function Bit 8, 9: bottom 2 bits of interrupt vector Bit 10, 11, 12: interrupt level IRQ 1..7, 0 = interrupts blocked Bit 13, 14, 15: top 3 bits of interrupt vector
+ F0 H	Interrupt enable register	read/write	2 bytes	Selection interrupt enable and –function input e18 Bit D8: 1 = interrupt released 0 = interrupt blocked Bit D9: 1 = rising edge 0 = falling edge Bit D10: 1 = interrupt exist (read only!) 0 = no interrupt exist (read only!)
+ F2 H	Interrupt enable register	read/write	2 bytes	Selection interrupt enable and –function input e20. Meaning of bits identical to input e18 (+ F0 H).
+ F4 H	Interrupt enable register	read/write	2 bytes	Selection interrupt enable and –function input e22. Meaning of bits identical to input e18 (+ F0 H).
+ F6 H	Interrupt enable register	read/write	2 bytes	Selection interrupt enable and –function input e24. Meaning of bits identical to input e18 (+ F0 H).
+ F8 H	Interrupt enable register	read/write	2 bytes	Selection interrupt enable and –function input e26. Meaning of bits identical to input e18 (+ F0 H).
+ FA H	Interrupt enable register	read/write	2 bytes	Selection interrupt enable and –function input e28. Meaning of bits identical to input e18 (+ F0 H).
+ FC H	Interrupt enable register	read/write	2 bytes	Selection interrupt enable and –function input e30. Meaning of bits identical to input e18 (+ F0 H).
+ FE H	Interrupt enable register	read/write	2 bytes	Selection interrupt enable and –function input e32. Meaning of bits identical to input e18 (+ F0 H).

4 Connector Layout

- Layout of VMEbus Connector P1 (Position X1)

Contact No.:	Signal names Row a	Row b	Row c
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5*
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12 V	+ 5 V STDBY	+12 V
32	+ 5 V	+ 5 V	+ 5 V

96-pin multipoint connector P1 (top)

□ DEP 232.1 connector layout

Connection at connector

GND = 0 V, reference point for +5 V (UB5), +12V (UB12+) and -12V (UB12-)

- Layout of VMEbus Connector P2 (Position X2)

Contact No.:	Signal names	
	Row a	Row c
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17	□ SYNC *	
18		
19	□ SN0 1)	
20	□ SN1 1)	
21	□ SN2 1)	
22	□ SN3 1)	
23	□ SN4 1)	
24	□ MN0 1)	
25	□ MN1 1)	
26		
27		
28		
29		
30		
31		
32		
64-pin multipoint connector P2 (bottom)		

□ DEP 232.1 connector layout.

SYNC : Synchronization signal for DPU. It is activated by installing the jumper on VMEbus board J2.

SN0 ... SN4 : Location addressing

MN0, MN1 : Selection of "master or expansion subrack 1 to 3"

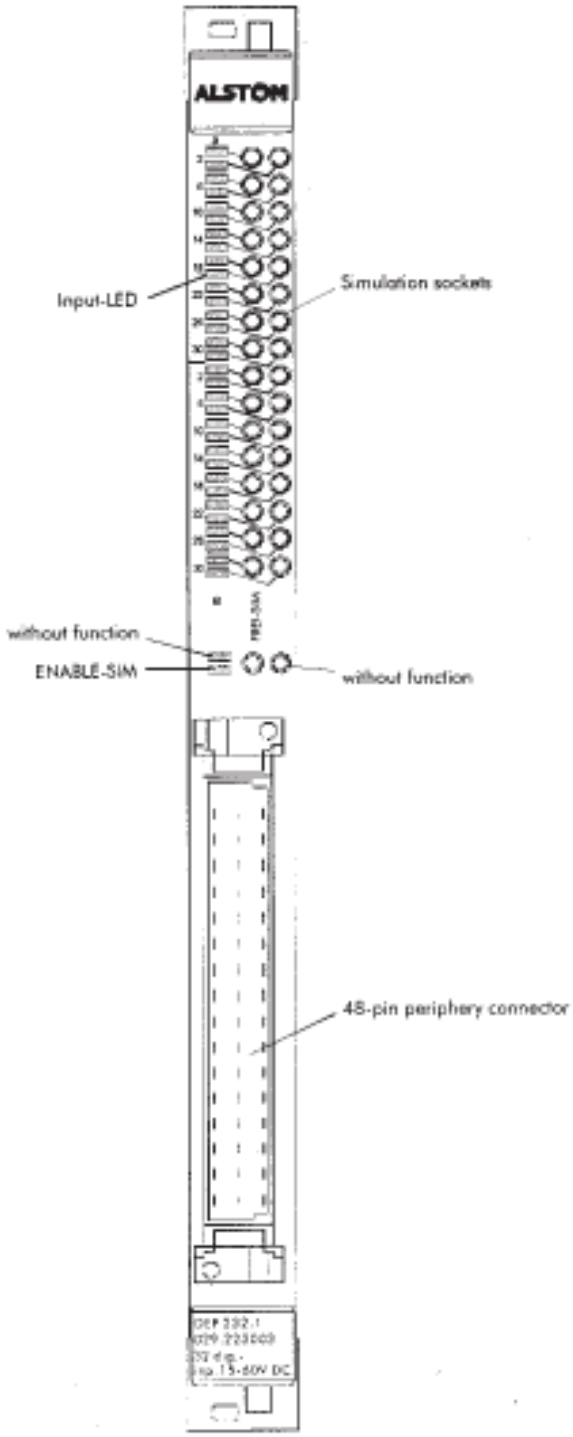
1) Signals are not continuously on the J2-VMEbus board. They are, instead, only connected to the connections *(see para. 2.1.1)*

- Periphery Connector Layout (Position X4)

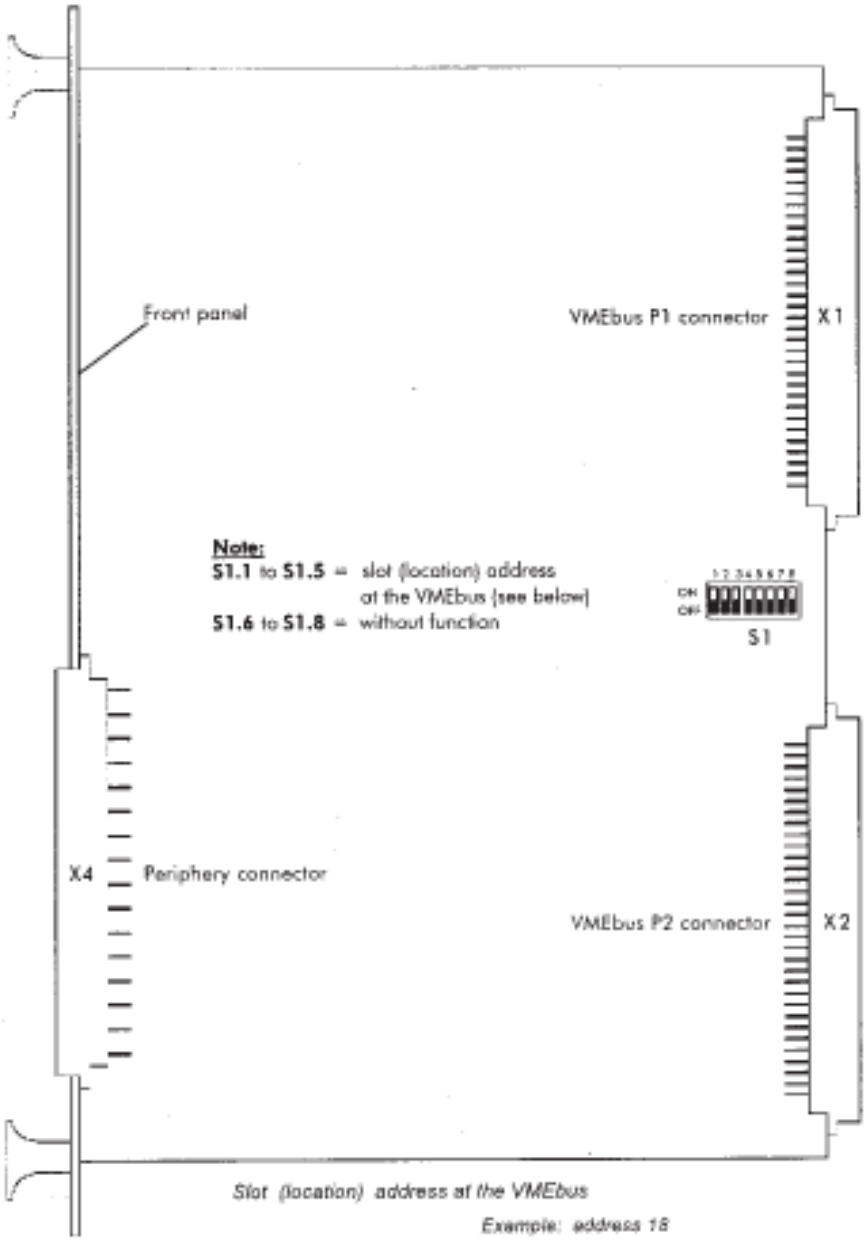
a32	Input 16	(group 2)	c32	MS1	(group 1)	e32	Input 32	(group 6)
a30	Input 15	(group 2)	c30			e30	Input 31	(group 6)
a28	Input 14	(group 2)	c28	MS2	(group 2)	e28	Input 30	(group 5)
a26	Input 13	(group 2)	c26			e26	Input 29	(group 5)
a24	Input 12	(group 2)	c24	MS3	(group 3)	e24	Input 28	(group 5)
a22	Input 11	(group 2)	c22			e22	Input 27	(group 4)
a20	Input 10	(group 2)	c20	MS4	(group 4)	e20	Input 26	(group 4)
a18	Input 9	(group 2)	c18			e18	Input 25	(group 4)
a16	Input 8	(group 1)	c16	MS5	(group 5)	e16	Input 24	(group 3)
a14	Input 7	(group 1)	c14			e14	Input 23	(group 3)
a12	Input 6	group 1)	c12			e12	Input 22	(group 3)
a10	Input 5	(group 1)	c10			e10	Input 21	(group 3)
a 8	Input 4	(group 1)	c 8	MS6	(group 6)	e 8	Input 20	(group 3)
a 6	Input 3	(group 1)	c 6			e 6	Input 19	(group 3)
a 4	Input 2	(group 1)	c 4			e 4	Input 18	(group 3)
a 2	Input 1	(group 1)	c 2			e 2	Input 17	(group 3)
48-pin multipoint connector (front panel)								

▮ ≙ Connection at plug connector (Control loop)

5 Front Panel



6 Assembly Diagram



Slot (location) address at the VMEbus

Example: address 18

OFF= 1-signal
ON = 0-signal

7 Use of the board

The following points must be observed for plant engineering when using the DEP 232.1:

- Wiring of the board
- Engineering with LogiCAD

7.1 Wiring of the board

Generally speaking, the plant wiring is carried out in such a manner that a pre-assembled connection unit - 48-pole connector with 2.2 m connection cable - and the following plug distributor (article No.: 029.209477) are located in the cubicle. The periphery is then connected to the plug connector.

7.2 Engineering with LogiCAD

With LogiCAD 3.1 and higher for DPU, the DEP 232.1 is permanently linked via the DEP/A modules for the inputs on the "a" row and the DEP/E to the inputs on the "e" row of the periphery connector in the I/O data chart.

Setting the input signal delay for X4e24 ... X4e32 inputs and disabling the internal enabling function of the simulation option is carried out via the rack configurator.

When using the DEP 232.1 in within Logidyn D2, synchronous mode (SYNC* synchronization signal available) is assumed.

In Logidyn D2, the interrupt functions described in section 3.5 are not supported and the input signal delay of inputs X4a..X4e22 is set at a constant value of t = 4 ms (op. class IV). Both are accessible via standard-language programs only.

8 Technical Specifications

POWER SUPPLY

VMEbus

UB5 = +5 V, ±3%
I ≤ 500 mA (all inputs with Ue1)
I ≤ 200 mA (all inputs with Ue0)

PERIPHERY (X4)

- Inputs a2 ... a32 and e2 ... e32

Ue1 = +12 V to +72 V
Ie 1 = 6 mA ± 30%
Ue0 = 0 V ... +5 V

MS1 ... MS6 = Reference point for input signals (see para. 2)

INPUTS DELAY

- Inputs a2 ... a32 and e2 ... e22: t = 4 ms (Op. class IV) or 0.5 ms (Op. class II), can be parameterized common for all input
- e24 ... e32: t = 4 ms (Op. class IV) or 0.5 ms (Op. class II), can be parameterized for every input

AMBIENT CONDITIONS

Ambient temperature	0° to + 55° C
Storage temperature	- 40° C to +85° C
Humidity	Class F

ELECTROMAGNETIC COMPATIBILITY (in DPU subrack)

- Standard (pr) EN 50081-2 for interference emissions
- Standard (pr) EN 50082-2 for interference resistance

MECHANICAL DESIGN

- INTERMAS format: 6 - 04
- Size / Dimensions: approx. 233.4 mm x 160 mm x 20.5 mm (H x D x W)
- Plug connectors
  - VMEbus P1: E96M-C1A, connections X1
  - VMEbus P2: E64M-C1A, connections X2
  - Periphery: E48M-C1A, connections X4
- Weight: approx. 500g

REORDER DATA

Type	DEP 232.1
Article No.	029.223003

ALSTOM

DAP 232
Output Board

Article No. 590.043150

ALSTOM Anlagen und Antriebssysteme GmbH
Culemeyerstr. 1, D-12277 Berlin, Tel.: +49 30 74 96-0, Fax: +49 30 74 96-21 09, email: postoffice.aas@ind.alstom.com

ALSTOM

Logidyn D2
DAP 232 Output Board

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Scope of validity:

ALSTOM Anlagen und
Antriebssysteme GmbH

Revision state

Rev.	Pages concerned	Remarks	Date	Designed Dept. / Name	Reviewed Dept. / Name	Approved Dept. / Name
02	all		07/96	E45 Fr. Klopsch	E45 Hr. Ullrich	E4 Dr. Groschupf
03	all, 2-1/5, 4-3/3	BG-No. new	03/97	E45 Fr. Klopsch	E45 Hr. Ullrich	E4 Dr. Groschupf
04	7-1/1	Chap. 7 new	02/98	E44 Fr. Klopsch	E47 Hr. Behrendt	E4 Dr. Groschupf
05	all	Logo new	01/99	E44 Fr. Klopsch	E47 Hr. Behrendt	E4 Dr. Groschupf

CONTENTS

1 General

The DAP 232 output board has 32 potential-free outputs which are overload-resistant and short-circuit-resistant.

The front panel is fitted with LEDs for the display of output signal states, as well as sockets for the simulation (1-signal) of the outputs by means of switching pins.

The DAP 232 is a VMEbus plug-in board of double Euroformat size (6 height units [HEs]) and of a width of 4 depth units [TEs].

2 Functional Description

The board contains 32 potential-free, high-active outputs which are divided into 4 groups of 8 outputs each. The groups are potential-isolated against each other and against the processing side (5V end, VMbus). Every group has its own periphery voltage supply and an enable input through which the outputs are activated.

The periphery (outputs, supply and enable signals) is connected via the 48-pin plug connector **X4** on the front panel. (The connector layout is compatible with the DAP 085 board).

The following chart shows the allocation of enable inputs and outputs and the power supply of the groups:

Enable inputs	Power supply		Outputs
	USx	MSx	
Fext 1 (X4c30)	US1 X4c16	MS1 X4c32	outputs 1 ... 8 (group 1), X4a2 ... X4a16
Fext 2 (X4c26)	US2 X4c14	MS2 X4c28	outputs 9 ... 16 (group 2), X4a18 ... X4a32
Fext 3 (X4c22)	US3 X4c8	MS3 X4c24	outputs 17 ... 24 (group 3), X4e2 ... X4e16
Fext 4 (X4c18)	US4 X4c6	MS4 X4c20	outputs 25 ... 32 (group 4), X4e18 ... X4e32

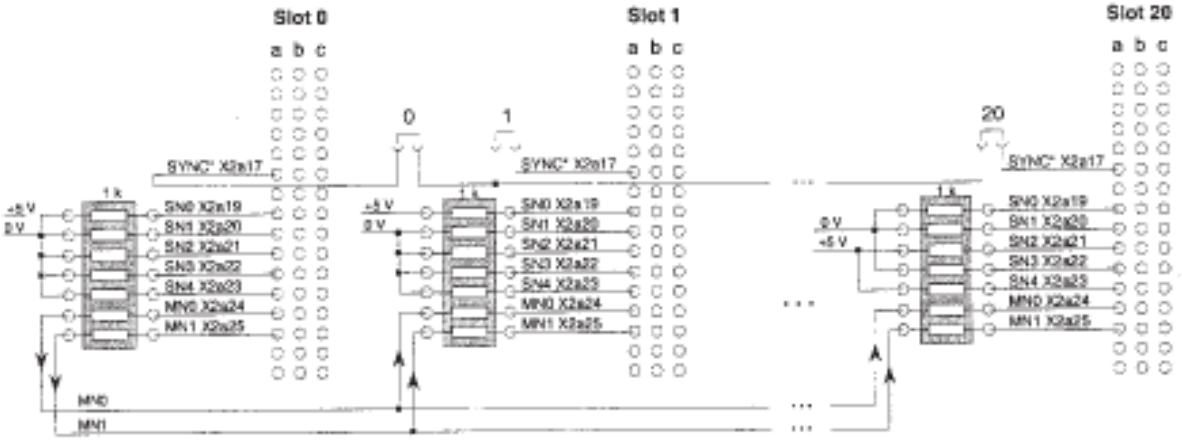
2.1 Addressing

The board has a VMEbus slave interface. It uses a 1-kByte address space in the A24:D16 address area. It is designed for use in the DPU (Decentralized Processing Unit) subrack, but it may also be used in the standard VMEbus subrack..

2.1.1 Basic Address in the DPU

In a DPU, the slots of the J2-VMEbus board have absolute location (slot) addresses from slot 0 to slot 20. The slots are addressed via the "a" row of the plug connector on the J2-VMEbus board. Resistance networks (1 kΩ switched to +5 V and 0 V) permit a binary-coded number of 0...20 (*SN0* ... *SN4*) to be adjusted for every slot, whilst another two connections (*MN0, MN1*) permit the definition of the subrack (master or expansion subrack).

The J2-VMEbus board in the DPU has the following structure with regard to SN0 ... SN4 and MN0, MN1 and the SYNC* signal:



With this layout, the DAP 232 can be used and addressed in the master subrack or in the three expansion subracks.
The DAP 232 generates the following basic addresses on the basis of the slot (location) addresses:

Slot	Master		Expansion board 1		Expansion board 2		Expansion board 3	
	Board address	Internal basic address	Board address	Internal basic address	Board address	Internal basic address	Board address	Internal basic address
0	0	E40000 H	21	E48000 H	42	E50000 H	63	E58000 H
1	1	E40400 H	22	E48400 H	43	E50400 H	64	E58400 H
2	2	E40800 H	23	E48800 H	44	E50800 H	65	E58800 H
3	3	E40C00 H	24	E48C00 H	45	E50C00 H	66	E58C00 H
4	4	E41000 H	25	E49000 H	46	E51000 H	67	E59000 H
5	5	E41400 H	26	E49400 H	47	E51400 H	68	E59400 H
6	6	E41800 H	27	E49800 H	48	E51800 H	69	E59800 H
7	7	E41C00 H	28	E49C00 H	49	E51C00 H	70	E59C00 H
8	8	E42000 H	29	E4A000 H	50	E52000 H	71	E5A000 H
9	9	E42400 H	30	E4A400 H	51	E52400 H	72	E5A400 H
10	10	E42800 H	31	E4A800 H	52	E52800 H	73	E5A800 H
11	11	E42C00 H	32	E4AC00 H	53	E52C00 H	74	E5AC00 H
12	12	E43000 H	33	E4B000 H	54	E53000 H	75	E5B000 H
13	13	E43400 H	34	E4B400 H	55	E53400 H	76	E5B400 H
14	14	E43800 H	35	E4B800 H	56	E53800 H	77	E5B800 H
15	15	E43C00 H	36	E4BC00 H	57	E53C00 H	78	E5BC00 H
16	16	E44000 H	37	E4C000 H	58	E54000 H	79	E5C000 H
17	17	E44400 H	38	E4C400 H	59	E54400 H	80	E5C400 H
18	18	E44800 H	39	E4C800 H	60	E54800 H	81	E5C800 H
19	19	E44C00 H	40	E4CC00 H	61	E54C00 H	82	E5CC00 H
20	20	E45000 H	41	E4D000 H	62	E55000 H	83	E5D000 H
	$\overline{MN0}$ & $\overline{MN1}$		MN0 & $\overline{MN1}$		$\overline{MN0}$ & MN1		MN0 & MN1	

Subrack selection:

$\overline{MN0}$ or $\overline{MN1}$ ≙ 0-signal
MN0 or MN1 ≙ 1-signal

Slot 0:

This slot is reserved for VCM 232 (master subrack) or VCS 232 (expansion subrack).

2.1.2 Basic Address for VMEbus Subrack without DPU

The slot (location) address for the generation of the basic address can be adjusted on the DAP 232:

- by suitable plug connector wiring if P2 plug connectors are available;
- internally on the DAP 232 by means of DIP switch S1.

In the case of the plug connector wiring, a binary coded number of 0 ... 20 (slots 0...20) is wired via the connectors X2a19 ... X2a23. The 1-signal is generated by connection to +5V, whilst the 0-signal is generated by connection to 0V (GND) (SN0 = 2^0, SN1 = 2^1, SN2 = 2^2, SN3 = 2^3, SN4 = 2^4). The same applies to the rack selection MN0/MN1.

Adjustment by means of DIP switch S1 is necessary if the DAP 232 is use in a subrack without a P2 plug connector.

Adjusting the slot (location) address:

	S1 - 1	^=	2^0
	S1 - 2	^=	2^1
	S1 - 3	^=	2^2
	S1 - 4	^=	2^3
	S1 - 5	^=	2^4
Position	„ON"	^=	0-signal
	„OFF"	^=	1-signal

2.2 Address Modifier

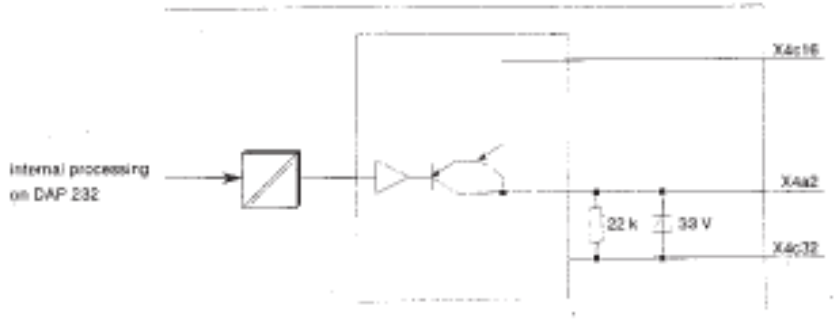
The DAP 232 only responds to user and supervisor data accesses with AM codes (AM0 ... AM5) for the A24:D16 area (standard). 39H or 3DH can be preset as AM codes.

BERR* is output in the event of an access to the DAP 232 in A24:D16 with LWORD* active. This also applies to an attempt to write into the identification register.

2.3 Outputs

The DAP 232 has 32 potential-free, current-source outputs which are overload-resistant and short-circuit-resistant. All outputs have the following structure:

e.g. **output 1**



Output amplifier TDE 1798
(SGS-Thomson)

2.3.1 Enabling the Output Groups

The output groups can be enabled either externally with Fext 1 to Fext 4, or internally via the command register *(see para. 3.1)* which is set via the VMEbus.

Internally or externally enabled output groups are signalled by the green LEDs "F1" to "F4". In the case of those output groups which are not enabled, the LEDs go on briefly when the UB5 supply voltage is connected; this has no influence on the enabling function.

Whenever the enable signals are interrupted (temporarily not available), or whenever the periphery supply voltages US 1 to US 4 are interrupted, the output register allocated to the groups are reset, so that the outputs are deactivated (0-signal). When the periphery supply voltages are connected again, or when the output groups are enabled again, the outputs of the corresponding groups have a 0-signal until the outputs are triggered via the VMEbus again.

2.3.2 Output Activation

The command register *(see para. 3.1)* permits the reactivation of the outputs for VMEbus tripping operations (in which case the enable signals of the output groups are active), or it permits the dominant reset (0-signal) of the outputs.
The simulation does not depend on the activation of the outputs.

2.3.3 Overload and Short-Circuit Protection of Outputs

All outputs are protected against overload/short-circuit. In the event of an overload/short-circuit condition, the output affected is switched off and the LED, which is associated to this output, blinks on the front panel. The fault is additionally indicated by the LED ("ALARM" LED) on the front panel, and bit 10 *(see para. 3.3)* is set in the status register.

After the fault (overload/short-circuit) has been cleared, a switching pin can be inserted into the "ALA.-RES." socket, or the command register *(see para,. 3.1)* can be tripped by the software in order to reset the internal error memories allocated to the outputs and to reset bit 10 of the status register *(see para. 3.3)*.

As it is not possible to reset the corresponding registers in the data dialog register in the case of an overload and/or short-circuit condition of outputs, outputs which have been tripped are activated automatically after the problem has been eliminated.

2.3.4 Display and Simulation of Output Signals

The front panel provides, for all outputs, LEDs and simulation possibilities for the output signals. Active process signals (1-signal) or simulated process signals are indicated by a green LED which is then lit.

The output signals (1-signal only) are simulated by inserting switching pins into the sockets allocated to the outputs, however, subject to the condition that the simulation function has been enabled.

This is achieved for all outputs together by inserting a switching pin into the "FREI-SIM" (ENABLE SIM) sokket and by the setting of the simulation enable flag in the command register *(see para. 3.1)*. The output signals cannot be simulated if the bit is deleted (reset) in the command register.

The red "FREI-SIM" LED signals the enabled condition of the simulation function. The LED goes on briefly when the supply voltage is connected.

2.4 Functional Control of the DAP 232

The following functions can be determined via the command register *(see para. 3.1)*.:

- **Start bit**

  After a SYSRESET* or after the connectionn of the supply voltage (UB5), the board is inactive with regard to VMEbus tripping (simulation is possible)!

- **Asynchronous or synchronous mode**

  The DAP 232 can work in the asynchronous and synchronous modes. In the asynchronous mode, the outputs are directly passed on to the periphery at the moment of writing. In the synchronous mode, however, the outputs are temporarily stored and not passed on to the periphery until the next falling edge of the synchronization signal SYNC* (X2a17). The outputs then remain stable until the next SYNC*. The changing from one mode to the other is performed by the software via the command register. If the synchronous mode has been preselected, and if the synchronization signal SYNC* fails to arrive within $t \leq 10ms$, the board automatically changes to the asynchronous mode.

- **Permanent or short-time storage**

  In the case of the permanent storage mode, the output signal states are retained from output to output. In the case of the short-time storage mode, the outputs are reset after the output after t = 130 ms, unless another output takes place during this time.

2.5 EMC Register

The EMC sensor on the board measures the electromagnetic, alternating field to which the board is exposed.

Level 1 responds in the event of a standard fault level III according to IEC 801-4, where the reliable operation of the board is still ensured under laboratory conditions. However, this message must already be regarded as a warning.

Level 2 responds in the event of a standard fault level IV according to IEC 801-4, where the reliable operation of the board is no longer ensured. This message must be regarded as a fault signal.

Bit 6 and bit 7 *(see para. 3.3)* of the status register indicate the degree of EMC exposure.

3 Dialog Registers

The dialog with the VMEbus is handled via these registers in the following manner:

Basic address	Access	Data size	Remarks
+ 0 H	write only	2 bytes	Command register, *see para. 3.1*
+ 2 H	read only	2 bytes	Acknowledgement register, *see para. 3.2*
+ 4 H	read only	2 bytes	Status register, *see para. 3.3*
+ 6 H	read only	2 bytes	Fault code register (0x0)
+ 8 H	read only	8 char	Identification, basic board type **DAP 232**
+ 10 H	read only	8 char	Identification, basic board type **DAP 232**
+ 18 H	read only	4 char	Identification, manufacturer **eac**
+ 1C H	read only	10 char	Identification, article No. 590.043150
+ 26 H	read only	2 char	Identification, revision code (0x0)
+ 28 H	read only	4 char	Identification, date of manufacture, e.g. 0595 (05th week 1995)
+ 2C H	read only	8 char	Identification, serial No. (e.g. 0000 2051)
+ 34 H	read only	8 char	Identification, firmware version (0x0)
+ 3C H	read only	2 bytes	Identification, assembly variant 0x0020
+ 3E H	read only	2 bytes	Identification, free description (0x0)
+ 100 H	read only	2 bytes	Read back binary outputs, "a"-row
+ 102 H	read only	2 bytes	Read back binary outputs, "e"-row
+ 104 H	read only	2 bytes	Mirror image of basic address + 100 H
+ 106 H	read only	2 bytes	Mirror image of basic address + 102 H
+ 108 H	write only	2 bytes	Write binary outputs, "a"-row
+ 10A H	write only	2 bytes	Write binary outputs, "e"-row
+ 10C H	write only	2 bytes	Mirror image of basic address + 108 H
+ 10E H	write only	2 bytes	Mirror image of basic address + 10A H
+ 110 H	write only	2 bytes	Set single bit, "a"-row (1 = set)
+ 112 H	write only	2 bytes	Set single bit, "e"-row (1 = set)
+ 114 H	write only	2 bytes	Mirror image of basic address + 110 H
+ 116 H	write only	2 bytes	Mirror image of basic address + 112 H
+ 118 H	write only	2 bytes	Delete single bit, "a"-row (1 = delete)
+ 11A H	write only	2 bytes	Delete single bit, "e"-row (1 = delete)
+ 11C H	write only	2 bytes	Mirror image of basic address + 118 H
+ 11E H	write only	2 bytes	Mirror image of basic address + 11A H

3.1 Command Register

The following functions are implemented in the command register:

Bit No.	Description	Action	Remarks
0			0
1			0
2			0
3			0
4	Acknowledge fault message	static	Reset bit 6, 7 and 10 in the status register
5	Start bit	Edge 0 → 1	for VMEbus tripping only
6			0
7			0
8	Mode of operation	static	1 = asynchronous 0 = synchronous
9	Simulation	static	1 = enabled 0 = disabled
10	Activate outputs	static	1 = outputs active 0 = outputs reset
11	Permanent storage	static	1 = permanent storage 0 = short-time storage
12	Enable group a2 ... a16	static	1 = internal enable 0 = external enable
13	Enable group a18 ... a32	static	1 = internal enable 0 = external enable
14	Enable group e2 ... e16	static	1 = internal enable 0 = external enable
15	Enable group e18 ... e32	static	1 = internal enable 0 = external enable

Explanations:

Bit 4 : Reset of the fault memory by the software.

Bit 5 : See "start bit" *(para. 2.4)*.

Bit 6 : See "asynchronous or synchronous mode " *(para. 2.4)*.

Bit 9 : See "simulation of output signals" *(para. 2.3.4)*.

Bit 10 : See "output activation" *(para. 2.3.2)*.

Bit 11 : See "permanent or short-time storage" *(para. 2.4)*.

Bit 12 : ... Bit 15 : See "enabling the output groups" *(para. 2.3.1)*.

SYSRESET* or the connection of the supply voltage (UB5) deletes the bits 0 to 8 and 10 to 15 of the command register (0-signal) and sets bit 9 to 1-signal.

3.2 Acknowledgement Register

The following bits of the command register are acknowledged in the acknowledgement register of the DAP 232:

Bit No.	Description	Remarks	
0		0	
1		0	
2		0	
3		0	
4	Fault message	1 = acknowledgement performed *(see para 3.1)*	
5	Start bit	1 = after the presetting of the start bit	0 = after a SYSRESET or after a power-on
6		0	
7		0	
8	Mode of operation	1 = asynchronous	0 = synchronous
9	Simulation	1 = simulation enabled	0 = simulation disabled
10	Outputs active	1 = outputs active	0 = outputs reset
11	Permanent storage	1 = permanent storage	0 = short-time storage
12	Enable group a2 ... a16	1 = internal or external enable	
13	Enable group a18 ... a32	1 = internal or external enable	
14	Enable group e2 ... e16	1 = internal or external enable	
15	Enable group e18 ... e32	1 = internal or external enable	

3.3 Status Register

The following messages are available in the status register of the DAP 232:

Bit No.	Description	Remarks	
0	Initialization	1 = Initialization underway	0 = board completely initialized
1		0	
2		0	
3		0	
4		0	
5		0	
6	Warning EMC sensor	1 = EMC level 1 exceeded	0 = ok.
7	Warning EMC sensor	1 = EMC level 2 exceeded	0 = ok.
8	Synchro clock SYNC* (P2 connector)	1 = Synchro clock t > 10 ms	0 = synchro clock t ≤ 10 ms
9	Simulation	1 = Simulation active	0 = Simulation disabled
10	Overload/output short-circuit	1 = at least 1 output overloaded	0 = outputs ok.
11	VME access [1]	1 = VME access t > 130 ms (Time out)	0 = accesses t ≤ 130 ms
12	Monitoring of external voltage	1 = supply error, at least 1 group	0 = supply ok. for all groups
13		0	
14		0	
15		0	

1) only valid for write accesses to the data dialog register (output register)

3.4 Data Dialog Register

This register is used for the setting of outputs and/or permits the reading back of the output states.

Basic address	Description	Access	Size	Remarks
+ 100 H	Binary outputs, "a"-row	read only	2 bytes	Read back D00 = a02, ... , D15 = a32
+ 102 H	Binary outputs, "e"-row	read only	2 bytes	Read back D00 = e02, ... , D15 = e32
+ 104 H	Binary outputs, "a"-row	read only	2 bytes	Mirror image of basic address +100 H
+ 106 H	Binary outputs, "e"-row	read only	2 bytes	Mirror image of basic address +102 H
+ 108 H	Binary outputs, "a"-row	write only	2 bytes	Write D00 = a02, ... , D15 = a32
+ 10A H	Binary outputs, "e"-row	write only	2 bytes	Write D00 = e02, ... , D15 = e32
+ 10C H	Binary outputs, "a"-row	write only	2 bytes	Mirror image of basic address +108 H
+ 10E H	Binary outputs, "e"-row	write only	2 bytes	Mirror image of basic address +10A H
+ 110 H	Set individual bit, "a"-row	write only	2 bytes	D00 = a02, ... , D15 = a32; 1 = set
+ 112 H	Set individual bit, "e"-row	write only	2 bytes	D00 = e02, ... , D15 = e32; 1 = set
+ 114 H	Set individual bit, "a"-row	write only	2 bytes	Mirror image of basic address +110 H
+ 116 H	Set individual bit, "e"-row	write only	2 bytes	Mirror image of basic address +112 H
+ 118 H	Delete individual bit, "a"-row	write only	2 bytes	D00 = a02, ... , D15 = a32 ; 1 = delete
+ 11A H	Delete individual bit, "e"-row	write only	2 bytes	D00 = e02, ... , D15 = e32; 1 = delete
+ 11C H	Delete individual bit, "a"-row	write only	2 bytes	Mirror image of basic address +118 H
+ 11E H	Delete individual bit, "e"-row	write only	2 bytes	Mirror image of basic address +11A H

The address mirroring ensures that both Big-Endian and Little-Endian processors can read these double words directly and without swapping.

The output values written into the data dialog register can be read back under the basic addresses +100H ... +107H. These output values can differ from the signal states actually indicated, because the deactivation of previously set outputs as a consequence of overload/short-circuit conditions or simulated output signal states are not detected at this point. Bits 9 and 10 in the status register *(see para. 3.3)* contain information to this effect.

The internal target states for the outputs are written into the registers +108H ... +10F H. The registers +108H ... +10F H and +100H ... +107H are identical in the asynchronous mode. In the synchroncus mode, +100H and +107H show the actual status, whilst +108H and +10F H show the status which the outputs will have after the next SYNC* synchronization signal.

4 Connector Layout

- **Layout of VMEbus Connector P1 (Position X1)**

Signal names								
Contact No.		Row a			Row b			Row c
1	□	D00		□	BBSY*		□	D08
2	□	D01		□	BCLR*		□	D09
3	□	D02		□	ACFAIL*		□	D10
4	□	D03		□	BG0IN*	•	□	D11
5	□	D04		□	BG0OUT*	•	□	D12
6	□	D05		□	BG1IN*	•	□	D13
7	□	D06		□	BG1OUT*	•	□	D14
8	□	D07		□	BG1IN*	•	□	D15
9	□	GND		□	BG2OUT*	•	□	GND
10	□	SYSCLK		□	BG3IN*	•	□	SYSFAIL*
11	□	GND		□	BG3OUT*	•	□	BERR*
12	□	DS1*			BR0*		□	SYSRESET*
13	□	DS0*			BR1*		□	LWORD*
14	□	WRITE*			BR2*		□	AM5*
15	□	GND			BR3*		□	A23
16	□	DTACK*		□	AM0		□	A22
17	□	GND		□	AM1		□	A21
18	□	AS*		□	AM2		□	A20
19	□	GND		□	AM3		□	A19
20	□	IACK*		□	GND		□	A18
21	□	IACKIN*	•		SERCLK		□	A17
22	□	IACKOUT*	•		SERDAT		□	A16
23	□	AM4		□	GND		□	A15
24	□	A07			IRQ7*		□	A14
25	□	A06			IRQ6*		□	A13
26	□	A05			IRQ5*		□	A12
27	□	A04			IRQ4*		□	A11
28	□	A03			IRQ3*		□	A10
29	□	A02			IRQ2*		□	A09
30	□	A01			IRQ1*		□	A08
31		-12 V			+ 5 V STDBY			+12 V
32	□	+ 5 V		□	+ 5 V		□	+ 5 V

96-pin multipoint connector P1 (top)

□ DAP 232 connector layout

• Connection at plug connector
•

GND – 0 V, Reference point for +5 V (UB5)

- Layout VMEbus Connector P2 (Position X2)

Contact No.	Signal names Row a	Row c
1		
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16		
17	SYNC *	
18		
19	SN0 1)	
20	SN1 1)	
21	SN2 1)	
22	SN3 1)	
23	SN4 1)	
24	MN0 1)	
25	MN1 1)	
26		
27		
28		
29		
30		
31		
32		

64-pin multipoint connector P2 (bottom)

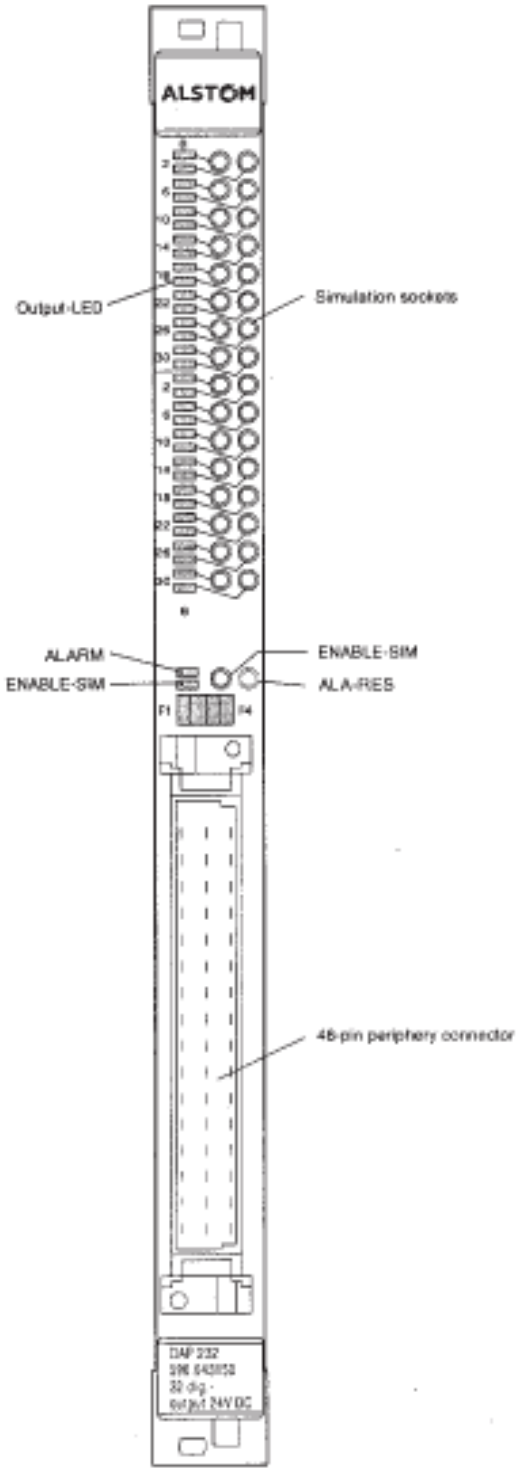
	DAP 232 connector layout.
SYNC :	Synchronization signal for DPU. It is activated by installing the jumper on P2.
SN0 ... SN4 :	As slot (location) address in the DPU magazine.
MN0, MN1 :	In the DPU, selection of "master magazine" or "expansion magazine 1 to 3".
1)	Signals are continuously on the J2-VMEbus board. They are, instead, only connected to the connections (see para. 2.1.1).

- **Layout of Periphery Connector (Position X4)**

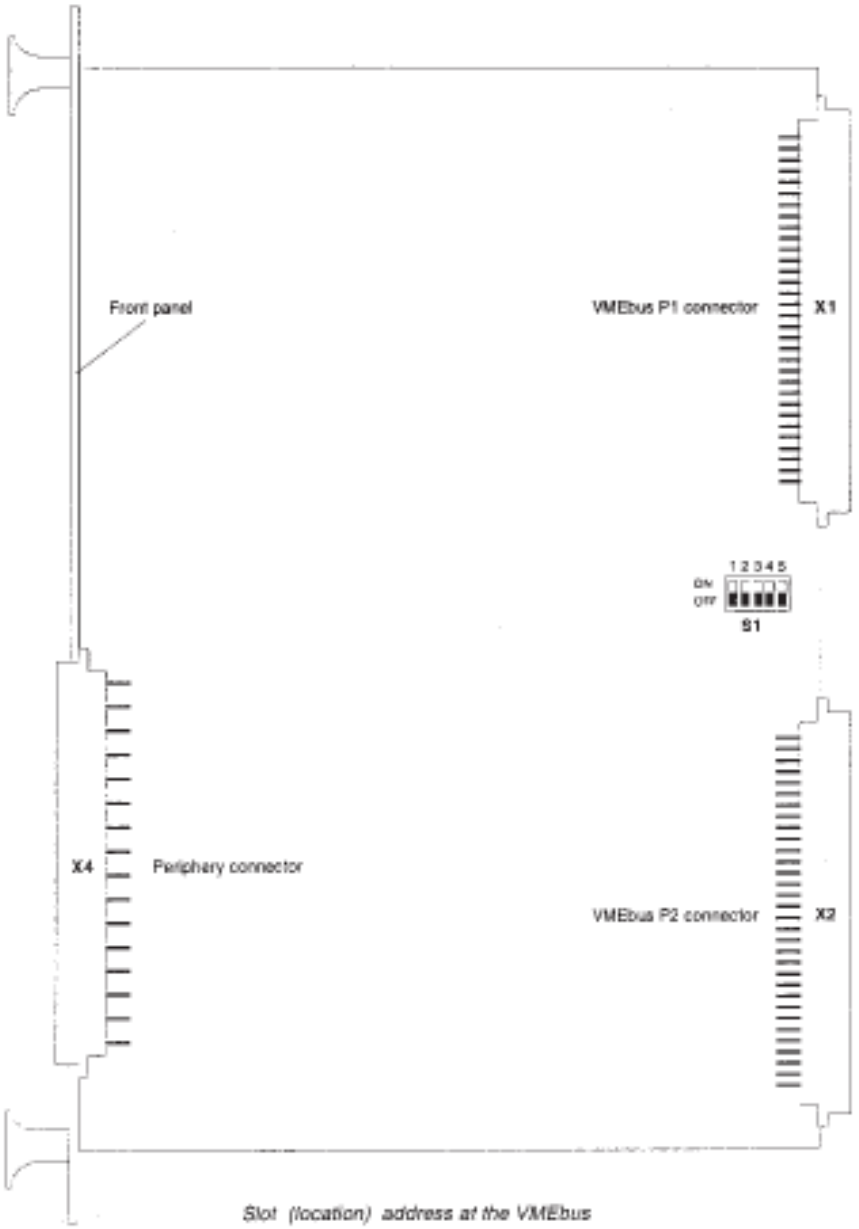
a32	Output 16	(group 2)	c32	MS1	(group 1)	e32	Output 32	(group 4)
a30	Output 15	(group 2)	c30	Fext 1	(group 1)	e30	Output 31	(group 4)
a28	Output 14	(group 2)	c28	MS2	(group 2)	e28	Output 30	(group 4)
a26	Output 13	(group 2)	c26	Fext 2	(group 2)	e26	Output 29	(group 4)
a24	Output 12	(group 2)	c24	MS3	(group 3)	e24	Output 28	(group 4)
a22	Output 11	(group 2)	c22	Fext 3	(group 3)	e22	Output 27	(group 4)
a20	Output 10	(group 2)	c20	MS4	(group 4)	e20	Output 26	(group 4)
a18	Output 9	(group 2)	c18	Fext 4	(group 4)	e18	Output 25	(group 4)
a16	Output 8	(group 1)	c16	US1	(group 1)	e16	Output 24	(group 3)
a14	Output 7	(group 1)	c14	US2	(group 2)	e14	Output 23	(group 3)
a12	Output 6	(group 1)	c12			e12	Output 22	(group 3)
a10	Output 5	(group 1)	c10			e10	Output 21	(group 3)
a 8	Output 4	(group 1)	c 8	US3	(group 3)	e 8	Output 20	(group 3)
a 6	Output 3	(group 1)	c 6	US4	(group 4)	e 6	Output 19	(group 3)
a 4	Output 2	(group 1)	c 4			e 4	Output 18	(group 3)
a 2	Output 1	(group 1)	c 2			e 2	Output 17	(group 3)
48-pin multipoint connector (front panel)								

⏐ ≙ Connection at plug connector (Control loop)

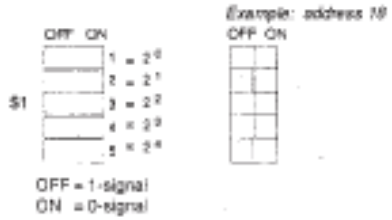
5 Front Panel



6 Assembly Diagram



Slot (location) address at the VMEbus



7 Use of the board

The following points must be observed for plant engineering when using the DAP 232:

- Wiring of the board
- Engineering with LogiCAD

7.1 Wiring of the board

Generally speaking, the plant wiring is carried out in such a manner that a pre-assembled connection unit - 48-pole connector with 2.2 m connection cable - and the following plug distributor (article No.: 029.209478) are located in the cubicle. The periphery is then connected to the plug connector.

7.2 Engineering with LogiCAD

With LogiCAD 3.1 and higher for DPU, the DAP 232 is permanently linked via the DAP/A modules for the inputs on the "a" row and the DAP/E to the inputs on the "e" row of the periphery connector in the I/O data chart.

Setting the output control (temporary / long-term saving), selecting the enabling for the output groups (internal/external) and disabling the internal enabling function of the simulation option is carried out via the DPU-KONF rack configurator.

When using the DAP 232 in a DPU under LogiCAD, synchronous mode (SYNC* synchronization signal available) is assumed.

8 Technical Specifications

POWER SUPPLY

VMEbus (X2)

	UB5	=	+5 V, ±3%
	I	≤	400 mA
	GND	=	0V, reference point for UB5

PERIPHERY (X4)

- **Outputs a2 ... a16**

Supply	US1	=	+24 V, +20% / -15%
	MS1	=	reference point for US1
	I	≤	30 mA (without output current)
Outputs			current source overload and short-circuit resistant
	Ua1	=	US1 - 1.3 V max.
	Ia1	≤	500 mA (max. current of all 8 outputs: Ia1=2A)
	Ia0	≤	0.1 mA
Input Fext 1	Ue1	=	+12 V to +29 V
	Ie1	=	6 mA ± 30%
	Ue0	=	0 V to +5 V
Switch-on (make) delay	t	=	200 µs

- **Outputs a18 ... a32**

Supply	US2	=	+24 V, +20% / -15%
	MS2	=	reference point for US2
	I	≤	30 mA (without output current)
Outputs			current source overload and short-circuit resistant
	Ua1	=	US2 - 1.3 V max.
	Ia1	≤	500 mA (max. current of all 8 outputs: Ia1=2A)
	Ia0	≤	0.1 mA
Input Fext 2	Ue1	=	+12 V to +29 V
	Ie1	=	10 mA ± 30%
	Ue0	=	0 V to +5 V
Switch-on (make) delay	t	=	200 µs

- **Outputs e2 ... e16**

Supply	US3	=	+24 V, +20% / -15%
	MS3	=	reference point for US3
	I	≤	30 mA (without output currenht)
Outputs			current source overload and short-circuit resistant
	Ua1	=	US3 - 1.3 V max.
	Ia1	≤	500 mA (max. current of all 8 outputs: Ia1=2A)
	Ia0	≤	0.1 mA
Input Fext 3	Ue1	=	+12 V to +29 V
	Ie1	=	10 mA ± 30%
	Ue0	=	0 V to +5 V
Switch-on (make) delay	t	=	200 µs

- **Outputs e16 ... e32**

Supply	US4	=	+24 V, +20% / -15%
	MS4	=	reference point for US4
	I	≤	30 mA (without output current)
Outputs			current source overload and short-circuit resistant
	Ua1	=	US4 - 1.3 V max.
	Ia1	≤	500 mA (max. current of all 8 outputs: Ia1=2A)
	Ia0	≤	0.1 mA
Input Fext 4	Ue1	=	+12 V to +29 V
	Ie1	=	10 mA ± 30%
	Ue0	=	0 V to +5 V
Switch-on (make) delay	t	=	200 µs

AMBIENT CONDITIONS

Ambient temperature	0° to + 55° C (with natural convection and a total level of all output currents of I < 4 A, or with forced ventilation at a rate of 0.5 m/s and a total level of all output currents of I < 8 A).
Storage temperature	- 40° C to +85° C
Humidity	Class F

ELECTROMAGNETC COMPATIBILITY (in the DPU subrack)

- Standard (pr) EN 50081-2 for interference emissions
- Standard (pr) EN 50082-2 for interference resistance

MECHANICAL DESIGN

- INTERMAS format

Size	6 - 04
Dimensions	approx. 233.4 mm x 160 mm x 20.5 mm (H x D x W)

- Plug connectors

VMEbus P1	E96M-C1A, connections X1
VMEbus P2	E64M-C1A, connections X2
Periphery	E48M-C1A, connections X4
Weight	approx. 500g

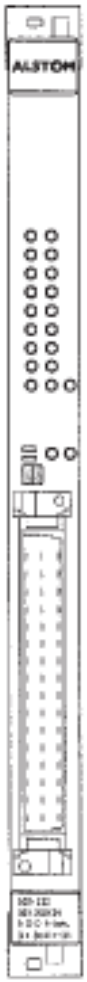
REORDER DATA

Type:	DAP 232
Article No.	590.043150

ALSTOM

ADA 232
Analog Input/Output Board
(Voltage Outputs)

Article No.: 029.202426



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Scope of validity:

ALSTOM Anlagen und
Antriebssysteme GmbH

Revision state

Rev.	Pages concerned	Remarks	Date	Designed Dept. / Name	Reviewed Dept. / Name	Approved Dept. / Name
00	all	new	07/97	E45 Fr. Klopsch	E44 Hr. Behrendt	E4 Dr. Groschupf
01	7-1/1	Revision	02/98	E45 Fr. Klopsch	E44 Hr. Behrendt	E4 Dr. Groschupf
02	all	Logo new	02/99	E44 Fr. Klopsch	E44 Hr. Behrendt	E4 Dr. Groschupf
03	27	Revision 4.88mA in 4.88mV	06/99	E44 Fr. Klopsch	E45 Hr. Behrendt	E4 Dr. Groschupf

CONTENTS

1 General

The ADA 232 is a VMEbus board designed for the input and output of analog signals with a resolution of 12 bits (11 bits plus the sign). The board is equipped with 8 potential-tied inputs; these inputs are designed as differential amplifiers with downstream filters with an input voltage range of Ue = +10 V ... 0 ... -10 V and 8 potential-tied output channels with an output voltage range of Ua = +10 V ... 0 ... -10 V.

The front panel features measuring sockets for all inputs and outputs - de-coupled via amplifiers.

The ADA 232 is a plug-in VMEbus board in double Euroformat (6 height units (HEs)) with a width of 4 divisions (TEs).

2 Functional Description

The board has 8 input channels with an input voltage range of Ue = +10 V ... 0 ... -10 V; the resolution of the converted values is 12 bits (11 bits plus the sign).

The inputs are potential-tied to each other and to the VMEbus processing function.

Connection to the periphery (analog inputs) is possible via the 48-pin **X4** connector on the front panel.

During each start up, the values of the 8 input channels are saved in the track/hold amplifiers. After this, the analog/digital conversion and storage for all 8 channels is carried out in the input register from which the values can be read *(see para. 3.4, Data Dialog Register)*.

All inputs are equipped with high-impedance, differential input amplifiers with an input impedance of Re $\geq$ 500 kΩ. The differential amplifiers serve to avoid potential propagation.

The differential input amplifiers are equipped with downstream anti-aliasing filters (2nd order) with a limit frequency of fg = 1 kHz. and where the outputs are connected to the analog/digital converters. The filtered input signals are also connected to the measuring sockets on the front panel via de-coupling amplifiers.

The board also features 8 digital/analog converters with a resolution of 12 bits (11 bits plus 1 bit digital sign) and an output voltage range of Ua = +10 V ... -10 V.

Connection to the periphery (analog outputs and enable inputs) is carried out via the 48-pin **X4** connector on the front panel.

The analog output channels are potential-tied with each other and with the VMEbus processing function.

A common enable control function is allocated to each four output channels. The voltage output can be enabled or disabled via this control function. The enable function can be activated either internally via the software or externally via the enable inputs. When the enable function is canceled, the output voltages of the relevant group are set at Ua = 0 V.

The following table shows the allocation of the external enable inputs to the output channels:

Enable inputs	Relevant reference point	Output channels
Fext 0 (X4c22)	MFext 0 (X4c24)	AOUT 0 ... 3 (Group 1) X4a18 ... X4a24
Fext 1 (X4c18)	MFext 1 (X4c20)	AOUT 4 ... 7 (Group 2) X4a26 ... X4a32

The enable inputs are potential isolated in relation to each other, to the output channels and to the VMEbus processing function. Each enable input has its own reference point (MFext 0, MFext 1).

Measuring sockets are located on the front panel for the analog output channels. The voltage outputs at the measuring sockets are de-coupled from the output channels by amplifiers, so that in the event of a short circuit at the measuring socket, the voltages which are output remain unaffected.

The UB5 supply (VMEbus connector P1) passes through a DC/DC transformer which generates the $\pm$ 15 V voltages for analog processing (A/D converter, D/A converter, amplifier, etc.).

2.1 Addressing the Board

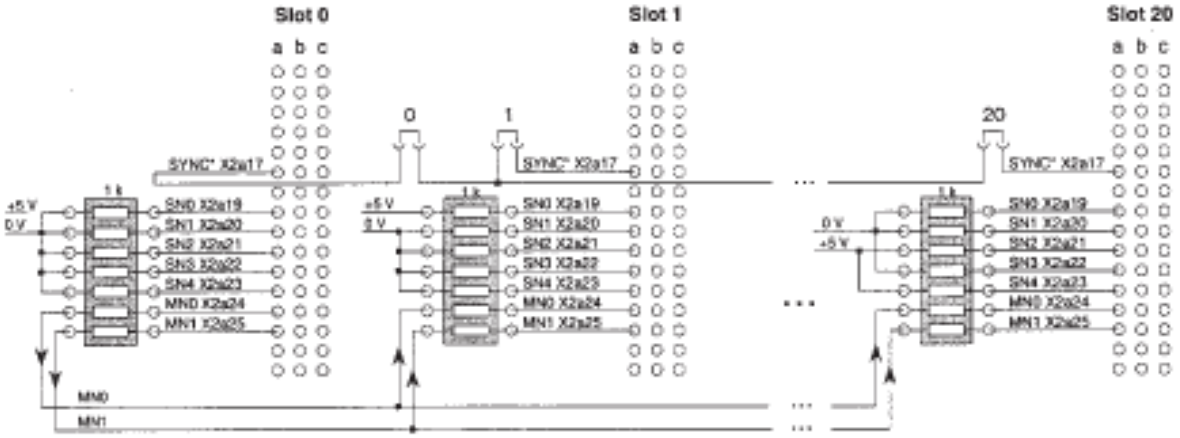
The board has one VMEbus slave interface and one address area of 1 kByte in the A24:D16 address area. It is provided for use in the DPU (Decentralized Processing Unit) subrack, however, it can also be used in standard VMEbus subracks.

When the ADA 232 is accessed and A24:D16 and LWORD* are active, BERR* is output, the same applies when an attempt is made to write in the identification register.

2.1.1 Base Address in the DPU

In a DPU , the slots on the J2 VMEbus board are subject to absolute location addressing, i.e. from slot 0 to slot 20. The location addressing is carried out via the "a" row of the plug connectors on the J2 VME bus board whilst a binary-coded number from 0 ... 20 *(SN0 ... SN4)* is set for each slot via resistance networks (1 kΩ switched after +5 V and 0 V) and the subrack (master or expansion subrack) is selected via two further connections *(MN0, MN1)*.

The following diagram shows the layout of the J2 VMEbus board in the DPU in the "a" row and with regard to the SN0 ... SN4, MN0, MN1 and the SYNC* signal:



This layout permits the ADA 232 to be used and addressed in the master subrack and in the three expansion subracks.
The ADA 232 forms the following base addresses from the location addressing:

Slot	Master		Expansion 1		Expansion 2		Expansion 3	
	Board address	Internal base address	Board address	Internal base address	Board address	Internal base address	Board address	Internal base address
0	0	E40000 H	21	E48000 H	42	E50000 H	63	E58000 H
1	1	E40400 H	22	E48400 H	43	E50400 H	64	E58400 H
2	2	E40800 H	23	E48800 H	44	E50800 H	65	E58800 H
3	3	E40C00 H	24	E48C00 H	45	E50C00 H	66	E58C00 H
4	4	E41000 H	25	E49000 H	46	E51000 H	67	E59000 H
5	5	E41400 H	26	E49400 H	47	E51400 H	68	E59400 H
6	6	E41800 H	27	E49800 H	48	E51800 H	69	E59800 H
7	7	E41C00 H	28	E49C00 H	49	E51C00 H	70	E59C00 H
8	8	E42000 H	29	E4A000 H	50	E52000 H	71	E5A000 H
9	9	E42400 H	30	E4A400 H	51	E52400 H	72	E5A400 H
10	10	E42800 H	31	E4A800 H	52	E52800 H	73	E5A800 H
11	11	E42C00 H	32	E4AC00 H	53	E52C00 H	74	E5AC00 H
12	12	E43000 H	33	E4B000 H	54	E53000 H	75	E5B000 H
13	13	E43400 H	34	E4B400 H	55	E53400 H	76	E5B400 H
14	14	E43800 H	35	E4B800 H	56	E53800 H	77	E5B800 H
15	15	E43C00 H	36	E4BC00 H	57	E53C00 H	78	E5BC00 H
16	16	E44000 H	37	E4C000 H	58	E54000 H	79	E5C000 H
17	17	E44400 H	38	E4C400 H	59	E54400 H	80	E5C400 H
18	18	E44800 H	39	E4C800 H	60	E54800 H	81	E5C800 H
19	19	E44C00 H	40	E4CC00 H	61	E54C00 H	82	E5CC00 H
20	20	E45000 H	41	E4D000 H	62	E55000 H	83	E5D000 H
	$\overline{MN0}$ & $\overline{MN1}$		MN0 & $\overline{MN1}$		$\overline{MN0}$ & MN1		MN0 & MN1	

Subrack selection:

$\overline{MN0}$ and/or $\overline{MN1}$ ≙ 0-signal
MN0 and/or MN1 ≙ 1-signal

Slot 0:

This slot is reserved for the VCM 232 (master subrack) or the VCS 232 (expansion subrack).

2.1.2 Base Address for the VMEbus subrack without a DPU

The location addressing required for generating the base address can be adjusted on the ADA 232 either:

- by connector wiring, when the P2 plug-in connectors are provided;
- or internally on the ADA 232 by the DIP switch S1.

In the case of the connector wiring, a binary-coded number, i.e. 0 .. 20 (slot 0 ... 20) is connected via the X2a19 ... X2a23 connections where the 1-signal is generated by a connection to +5 V and the 0-signal by a connection to 0 V (GND) (SN0 = 2^0, SN1 = 2^1, SN2 = 2^2, SN3 = 2^3, SN4 = 2^4). The same applies to the rack selection, i.e. MN0/MN1.

The DIP switch S1 is required for adjusting when the ADA 232 is used in a subrack without P2 plug-in connectors.

Adjusting the location addresses:

	S1 - 1	≙	2^0
	S1 - 2	≙	2^1
	S1 - 3	≙	2^2
	S1 - 4	≙	2^3
	S1 - 5	≙	2^4
Position	„ON"	≙	0-signal
	„OFF"	≙	1-signal

2.2 Address Modifier

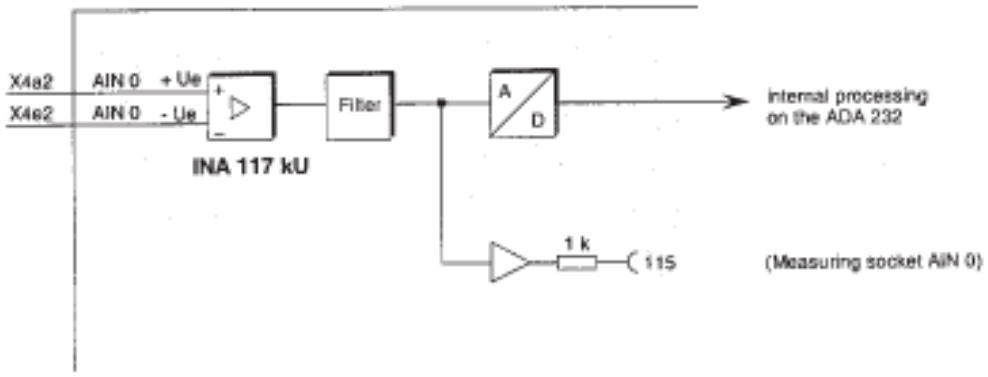
The ADA 232 responds only to user and supervisor access with AM codes (AM0 ... AM5) for the A24:D16 (standard) range where 39 H or 3D H can be specified.

2.3 Inputs

The ADA 232 is equipped with 8 differential amplifiers with an input impedance of Re ≥ 500 kΩ. Each amplifier comes with a downstream anti-aliasing filter with a limit frequency of fg = 1 kHz. Their outputs are connected to the analog/digital converters and to the measuring sockets via de-coupling amplifiers.

The layout of all outputs is as follows:

e.g. **Input 0:**

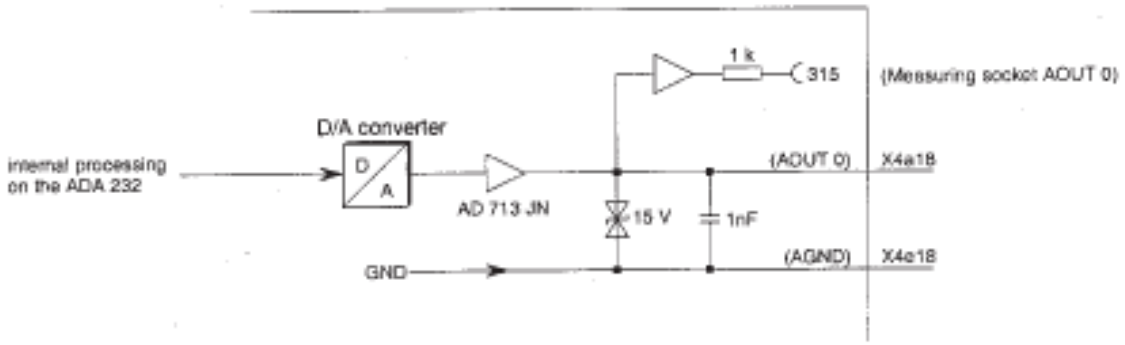


Note: +Ue positive -Ue ⇒ D15 = 0, VMEbus data word
+Ue negative -Ue ⇒ D15 = 1, VMEbus data word

2.4 Outputs

The layout of the analog outputs is as follows:

e.g. **Output 0**



2.4.1 Enabling the Analog Output Channels

The group-wise enabling of the output channels can be either externally carried out with Fext 0 and Fext 1 or internally via the command register *(see para. 3.1)* which is set via the VMEbus.

Each time enabling is interrupted (temporary cancellation of enabling), the output registers allocated to the group are reset in the data dialog register and the outputs are hence reset (Ua = 0 V). If the UB5 supply voltage and the subsequent switching fails, all outputs are reset. This status (Ua = 0 V) remains, even after the UB5 supply has been restored or the disrupted enabling has been reactivated, until new output values are specified via the VMEbus.
LEDs are located on the front panel which signal the enabling of output groups; these LEDs are lit when enabling has been activated either internally or externally.

2.4.2 Activating the Output Channels

Via the command register *(see para. 3.1)*, all outputs can be either activated, which means that the internal or external enabling is activated for the output channels, or dominantly reset (all output channels Ua = 0 V).

2.5 Function Control of the ADA 232

The following functions can be controlled via the command register *(see para. 3.1)*:

- **Startbit**

  After SYSRESET* , or after the supply voltage (UB5) has been switched on, the input signals can be read by the board after the initialization phase. All outputs from the VMEbus to the D/A converter are ignored until the start bit is set. Until then, the output channels have an output voltage of Ua = 0 V.

- **Asynchronous or Synchronous Mode**

  The ADA 232 can operate both in asynchronous and in synchronous mode.
  In asynchronous mode, the analog/digital conversion for all channels is started by a free-running clock generator and the converted digital values are written in the data dialog register. The outputs are directly passed on to the periphery as soon as they are written. In synchronous mode, the analog/digital conversion for all channels is started with the falling edge of SYNC* (X2a17), i.e. the synchronization signal. After conversion, the digital values are written in the data dialog register and remain stable until the next SYNC*. The outputs are temporarily stored, and are not passed on to the periphery until the next falling edge of the synchronization signal SYNC*. They then remain stable until the next SYNC*.
  Switching between the two modes is carried out in the software via the command register. If synchronous mode has been selected and the SYNC* synchronization signal does not arrive within $t \leq 10$ ms, the board automatically switches to asynchronous mode.

- **Long-term or Short-term Storage**

  In the case of long-term storage, the output voltages remain constant from output to output. In the case of short-term storage, after output of all set output voltages, Ua = 0 V is set after t = 130 ms, of no new output takes place within this period.

2.6 EMC Register

The EMC sensor on the board measures the electromagnetic alternating field to which the board is exposed.

Level 1 responds to a fault level III standardized according to IEC 801-4 where the board still works in a reliable manner under laboratory conditions. This message should, however, be understood as a warning.

Level 2 responds to a fault level IV standardized according to IEC 801-4 where perfect operation of the board is no longer ensured. This message must be understood as a fault message.

Bit 6 and bit 7 (*see para. 3.3*) from the status register show the degree of EMC interference.

3 Dialog Register

The dialog with the VMEbus is carried out via this register as follows:

Base address	Access	Data Size	Remarks
+ 0 H	write only	2 bytes	Command register, *see para. 3.1*
+ 2 H	read only	2 bytes	Acknowledgement register, *see para. 3.2*
+ 4 H	read only	2 bytes	Status register, *see para. 3.3*
+ 6 H	read only	2 bytes	Error code register (0x0)
+ 8 H	read only	8 char	Identification, basic board type: **ADA 232**
+ 10 H	read only	8 char	Identification, board type: **ADA 232**
+ 18 H	read only	4 char	Identification, manufacturer: **eac**
+ 1C H	read only	10 char	Identification, article No.: 029.202426
+ 26 H	read only	2 char	Identification, revision code (0x0)
+ 28 H	read only	4 char	Identification, date of manufacture, e.g. 0597 (5th calendar week 97)
+ 2C H	read only	8 char	Identification, Series No. (e.g. 0000 2051)
+ 34 H	read only	8 char	Identification, firmware version (0x0)
+ 3C H	read only	2 bytes	Identification, assembly variant 0x0010
+ 3E H	read only	2 bytes	Identification, free description (0x0)
+ 100 H ⋮ + 17E H	read/write ⋮ read/write	2 bytes ⋮ 2 bytes	Data dialog register: Register for input and output values. Mirroring of the values.

3.1 Command Register

The following functions are carried out in the command register:

Bit No.	Name	Action	Remarks
0			0
1			0
2			0
3			0
4	Acknowledge error message	static	Reset bit 6 and 7 in the status register
5	Start bit	Edge 0 → 1	Must be observed in the case of outputs from the VMEbus
6			0
7			0
8	Operating mode	static	1 = asynchronous 0 = synchronous
9			0
10	Activate output channels	static	1 = output channels active 0 = output channels reset (Ua = 0 V)
11	Output control	static	1 = long-term storage 0 = short-term storage
12	Enable AOUT 0 ... AOUT 3	static	1 = internal enabling 0 = external enabling
13	Enable AOUT 4 ... AOUT 7	static	1 = internal enabling 0 = external enabling
14			0
15			0

Explanation:

Bit 4 : Reset the error memory per software.

Bit 5 : Refer to start bit *(see para. 2.5)*.

Bit 8 : Refer to asynchronous or synchronous mode *(para. 2.5)*.

Bit 10 : Refer to activating the output channels *(para. 2.4.2)*.

Bit 11 : Refer to short-term or long-term storage (*para. 2.5)*.

Bit 12 : ... Bit 13 : Refer to enabling analog output channels *(para. 2.4.1)*.

The bits 0 to 15 (0-signal) are deleted in the command register by SYSRESET* or when the supply voltage (UB5) is switched on.

3.2 Acknowledgment Register

The following bits of the command register are reset in the acknowledgment register of the ADA 232:

Bit No.	Name	Remarks
0		0
1		0
2		0
3		0
4	Acknowledge error message	1 = Acknowledgment completed *(see para. 3.1)*
5	Start bit	1 = after start bit has been set 0 = after SYSRESET or supply ON
6		0
7		0
8	Operating mode	1 = asynchronous 0 = synchronous
9		0
10	Activating the output channels	1 = output channels active 0 = Output channels reset (Ua = 0 V)
11	Saving output channels	1 = long-term storage 0 = short-term storage
12	Enable AOUT 0 ... AOUT 3	1 = internal or external enabling
13	Enable AOUT 4 ... AOUT 7	1 = internal or external enabling
14		0
15		0

3.3 Status Register

The following messages are provided in the status register of the ADA 232:

Bit No.	Name	Remarks
0	Initialization	1 = Initialization running 0 = board is initialized
1		0
2		0
3		0
4		0
5		0
6	Warning EMC sensor	1 = EMC level 1 exceeded 0 =OK.
7	Warning EMC sensor	1 = EMC level 2 exceed 0 = OK.
8	Synchronous clock SYNC* (P2 connector)	1 = Synchronous clock t > 10 ms 0 = Synchronous clock t ≤ 10 ms
9		0
10		0
11	VME access [1]	1 = VME access t > 130 ms (timeout) 0 = access t ≤ 130 ms
12	Monitoring the supply +15 V/-15 V	1 = Supply +15 V or -15 V beyond tolerance 0 = Supply +15 V and -15 V OK.
13		0
14		0
15		0

1) applicable only for access to the data dialog register.

3.4 Data Dialog Register

Via this register, the values from the converter input voltages Ue can be read and the outputs can be set and/or read back.

Base address	Name	Access	Size	Remarks
+ 100 H	Input voltage channel 0 (AIN 0)	read only	2 bytes	See para. 3.4.1
+ 102 H			2 bytes	Not defined
+ 104 H	Input voltage channel 0 (AIN 0)	read only	2 bytes	Mirroring of the base address +100 H
+ 106 H			2 bytes	Not defined
+ 108 H	Input voltage channel 1 (AIN 1)	read only	2 bytes	See para. 3.4.1
+ 10A H			2 bytes	Not defined
+ 10C H	Input voltage channel 1 (AIN 1)	read only	2 bytes	Mirroring of the base address +108 H
+ 10E H			2 bytes	Not defined
+ 110 H	Input voltage channel 2 (AIN 2)	read only	2 bytes	See para. 3.4.1
+ 112 H			2 bytes	Not defined
+ 114 H	Input voltage channel 2 (AIN 2)	read only	2 bytes	Mirroring of the base address +110 H
+ 116 H			2 bytes	Not defined
+ 118 H	Input voltage channel 3 (AIN 3)	read only	2 bytes	See para. 3.4.1
+ 11A H			2 bytes	Not defined
+ 11C H	Input voltage channel 3 (AIN 3)	read only	2 bytes	Mirroring of the base address +118 H
+ 11E H			2 bytes	Not defined
+ 120 H	Input voltage channel 4 (AIN 4)	read only	2 bytes	See para. 3.4.1
+ 122 H			2 bytes	Not defined
+ 124 H	Input voltage channel 4 (AIN 4)	read only	2 bytes	Mirroring of the base address +120 H
+ 126 H			2 bytes	Not defined
+ 128 H	Input voltage channel 5 (AIN 5)	read only	2 bytes	See para. 3.4.1
+ 12A H			2 bytes	Not defined
+ 12C H	Input voltage channel 5 (AIN 5)	read only	2 bytes	Mirroring of the base address +128 H
+ 12E H			2 bytes	Not defined
+ 130 H	Input voltage channel 6 (AIN 6)	read only	2 bytes	See para. 3.4.1
+ 132 H			2 bytes	Not defined
+ 134 H	Input voltage channel 6 (AIN 6)	read only	2 bytes	Mirroring of the base address +130 H
+ 136 H			2 bytes	Not defined
+ 138 H	Input voltage channel 7 (AIN 7)	read only	2 bytes	See para. 3.4.1
+ 13A H			2 bytes	Not defined
+ 13C H	Input voltage channel 7 (AIN 7)	read only	2 bytes	Mirroring of the base address +138 H
+ 13E H			2 bytes	Not defined

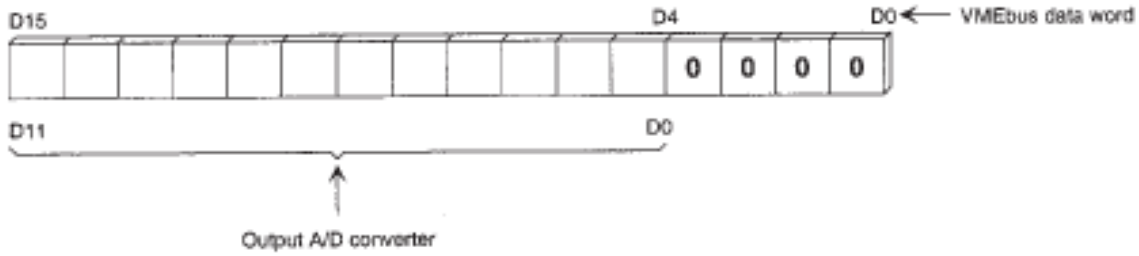
Base address	Name	Access	Size	Remarks
+ 140 H	Data preset for channel 0 (AOUT 0)	write/read	2 bytes	See para. 3.4.2
+ 142 H			2 bytes	Not defined
+ 144 H	Data preset for channel 0 (AOUT 0)	write/read	2 bytes	Mirroring of the base address +140 H
+ 146 H			2 bytes	Not defined
+ 148 H	Data preset for channel 1 (AOUT 1)	write/read	2 bytes	See para. 3.4.2
+ 14A H			2 bytes	Not defined
+ 14C H	Data preset for channel 1 (AOUT 1)	write/read	2 bytes	Mirroring of the base address +148 H
+ 14E H			2 bytes	Not defined
+ 150 H	Data preset for channel 2 (AOUT 2)	write/read	2 bytes	See para. 3.4.2
+ 152 H			2 bytes	Not defined
+ 154 H	Data preset for channel 2 (AOUT 2)	write/read	2 bytes	Mirroring of the base address +150 H
+ 156 H			2 bytes	Not defined
+ 158 H	Data preset for channel 3 (AOUT 3)	write/read	2 bytes	See para. 3.4.2
+ 15A H			2 bytes	Not defined
+ 15C H	Data preset for channel 3 (AOUT 3)	write/read	2 bytes	Mirroring of the base address +158 H
+ 15E H			2 bytes	Not defined
+ 160 H	Data preset for channel 4 (AOUT 4)	write/read	2 bytes	See para. 3.4.2
+ 162 H			2 bytes	Not defined
+ 164 H	Data preset for channel 4 (AOUT 4)	write/read	2 bytes	Mirroring of the base address +160 H
+ 166 H			2 bytes	Not defined
+ 168 H	Data preset for channel 5 (AOUT 5)	write/read	2 bytes	See para. 3.4.2
+ 16A H			2 bytes	Not defined
+ 16C H	Data preset for channel 5 (AOUT 5)	write/read	2 bytes	Mirroring of the base address +168 H
+ 16E H			2 bytes	Not defined
+ 170 H	Data preset for channel 6 (AOUT 6)	write/read	2 bytes	See para. 3.4.2
+ 172 H			2 bytes	Not defined
+ 174 H	Data preset for channel 6 (AOUT 6)	write/read	2 bytes	Mirroring of the base address +170 H
+ 176 H			2 bytes	Not defined
+ 178 H	Data preset for channel 7 (AOUT 7)	write/read	2 bytes	See para. 3.4.1
+ 17A H			2 bytes	Not defined
+ 17C H	Data preset for channel 7 (AOUT 7)	write/read	2 bytes	Mirroring of the base address +178 H
+ 17E H			2 bytes	Not defined

The purpose of the address mirroring is to ensure that both Big-Endian and Little-Endian processors can directly output such double words without swapping.

3.4.1 Allocation of the Analog / Digital Values

The board contains 8 bipolar analog / digital converters with a resolution of 12 bits; the highest bit (D11 from the A/D converter) determines the polarity of the input voltages.

The allocation between the data read in two's complement by the VMEbus and the triggering of the A/D converter is as follows:



$D0 = 2^0$

$D11 = 2^{11}$

D11 from the A/D converter determines the polarity of the converted input voltage:

D11 = 1, negative input voltage (+Ue negative - Ue)

D11 = 0, positive input voltage (+Ue positive - Ue)

0-signal is entered in the bits D0 ... D3 of the input register of the data dialog register (VMEbus data word).

The following table shows the digital values from the converter analog values at the VMEbus:

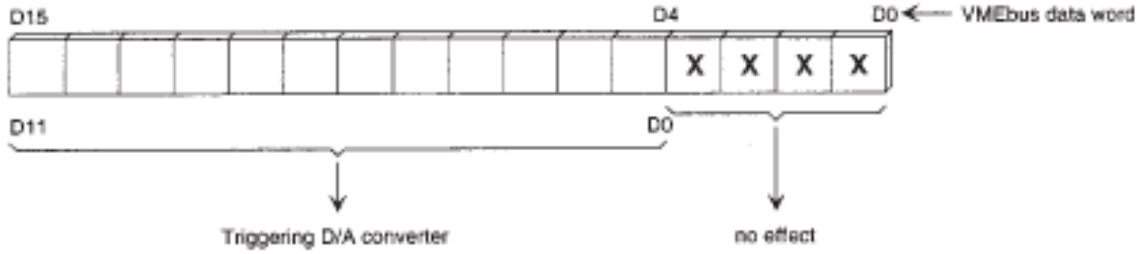
Digital Value *(VMEbus)* **Hex Value**	**Input voltage Ue**
7FF0	+ 10 V - 1LSB
7FE0	+ 10 V - 2LSB
⋮	
0010	+ 4.88 mV
0000	0 V
FFF0	- 4.88 mV
FFE0	- 9.76 mV
⋮	⋮
8020	- 10 V - 2LSB
8010	- 10 V - 1LSB
8000	- 10 V

1 LSB (least significant bit) = 4.88 mV

3.4.2 Allocation of the Digital / Analog Values

The board contains 8 bipolar digital / analog converters with a resolution of 12 bits; the highest bit (D15 from the VMEbus) determines the polarity of the output voltages.

The allocation between the data to be set in two's complement by the VMEbus and the triggering of the D/A converter is as follows:



D0 = 2^0

D11 = 2^{11}

D11 determines the polarity of the output voltage:

D11 = 1, negative output voltage

D11 = 0, positive output voltage

The following table shows the D/A conversion of the digital values (VMEbus):

Digital Value (*VMEbus*) Hex Value	Output voltage Ua
7FFx	+ 10 V - 1LSB
7FEx	+ 10 V - 2LSB
⋮	
001x	+ 4.88 mV
000x	0 V
FFFx	- 4.88 mV
FFEx	- 9.76 mV
⋮	⋮
802x	- 10 V - 2LSB
801x	- 10 V - 1LSB
800x	- 10 V

↑

x = any Hex value

1 LSB (least significant bit) = 4.88 mV

4 Connector Layout

- **VMEbus Connector Layout P1 (Position X1)**

Contact No.	Signal names Row a	Row b	Row c
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5*
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12 V	+5 V STDBY	+12 V
32	+5 V	+5 V	+5 V

96-pin multipoint connector P1 (top)

□ ADA 232 connector layout

Connection at the connector

GND = 0 V, reference point of +5 V (UB5)

- VMEbus Connector Layout P2 (Position X2)

Contact No.	Signal names Row a	Row b	Row c
1			
2			
3			
4			
5			
6			
7			
8			
9			
10			
11			
12			
13			
14			
15			
16			
17	☐ SYNC *		
18			
19	☐ SN0 1)		
20	☐ SN1 1)		
21	☐ SN2 1)		
22	☐ SN3 1)	☐ GND	
23	☐ SN4 1)		
24	☐ MN0 1)		
25	☐ MN1 1)		
26			
27			
28			
29			
30			
31			
32			
96-pin multipoint connector P2 (bottom)			

☐ ADA 232 connector layout.

SYNC * : Synchronization signal for DPU. It is activated by installing the jumper on VMEbus board J2.

SN0 ... SN4 : As slot (location) address in the DPU magazine.

MN0, MN1 : In the DPU, selection of "master magazine" or "expansion magazine 1 to 3".

GND : 0 V (M5), reference point of +5 V.

1) Signals are not continuously on the J2-VMEbus board. They are, instead, only connected to the connections *(see para. 2.1.1)*.

- **Periphery Connector Layout (Position X4)**

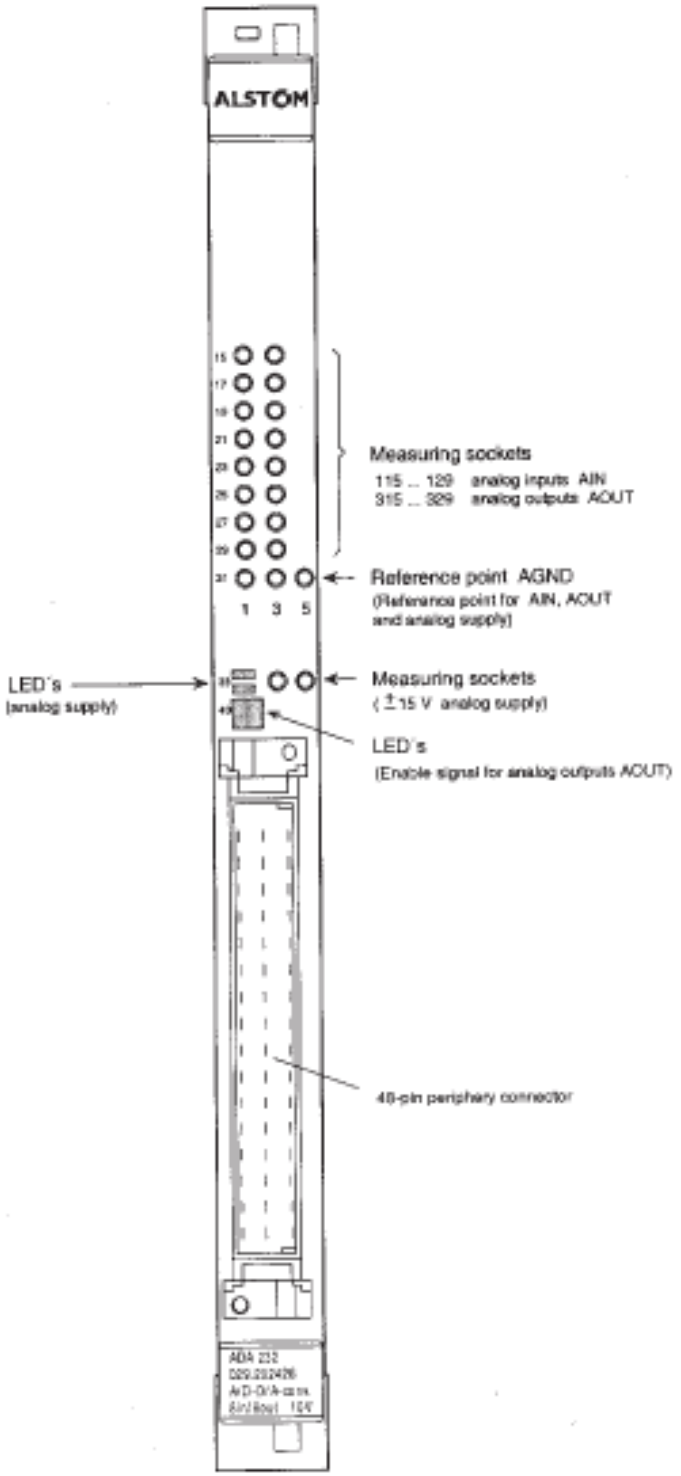
a32	AOUT 7 (Group 1)	c32		e32	AGND
a30	AOUT 6 (Group 1)	c30		e30	AGND
a28	AOUT 5 (Group 1)	c28		e28	AGND
a26	AOUT 4 (Group 1)	c26		e26	AGND
a24	AOUT 3 (Group 0)	c24	MFext 0 (M for Fext 0)	e24	AGND
a22	AOUT 2 (Group 0)	c22	Fext 0 (AOUT 0 to 3)	e22	AGND
a20	AOUT 1 (Group 0)	c20	MFext 1 (M for Fext 1)	e20	AGND
a18	AOUT 0 (Group 0)	c18	Fext 1 (AOUT 4 to 7)	e18	AGND
a16	AIN 7, +Ue	c16		e16	AIN 7, -Ue
a14	AIN 6, +Ue	c14		e14	AIN 6, -Ue
a12	AIN 5, +Ue	c12		e12	AIN 5, -Ue
a10	AIN 4, +Ue	c10		e10	AIN 4, -Ue
a 8	AIN 3, +Ue	c 8		e 8	AIN 3, -Ue
a 6	AIN 2, +Ue	c 6		e 6	AIN 2, -Ue
a 4	AIN 1, +Ue	c 4		e 4	AIN 1, -Ue
a 2	AIN 0, +Ue	c 2		e 2	AIN 0, -Ue
48-pin multipoint connector					

⋮ ≙ Connection at plug connector (Control loop)

Note:

A reference point AGND is allocated to each output channel AOUT 0 ... AOUT 7. This means that a twisted pair cable for analog processing can be laid for each output channel, hence reducing interference and preventing voltage errors in the voltage output resulting from voltage drops in the reference point supply cable.

5 Front Panel



5.1 Front Panel Elements

The coordinate captions must be read as follows:

⇒ **Numbers from the left**

1st digit	*indicates the columns*
2nd and 3rd digit	*indicates the lines*

⇒ **additionally for vertically arranged LEDs**

Coordinate with "A" supplement	^	*upper LED*
Coordinate with "B" supplement	^	*lower LED*

Measuring sockets

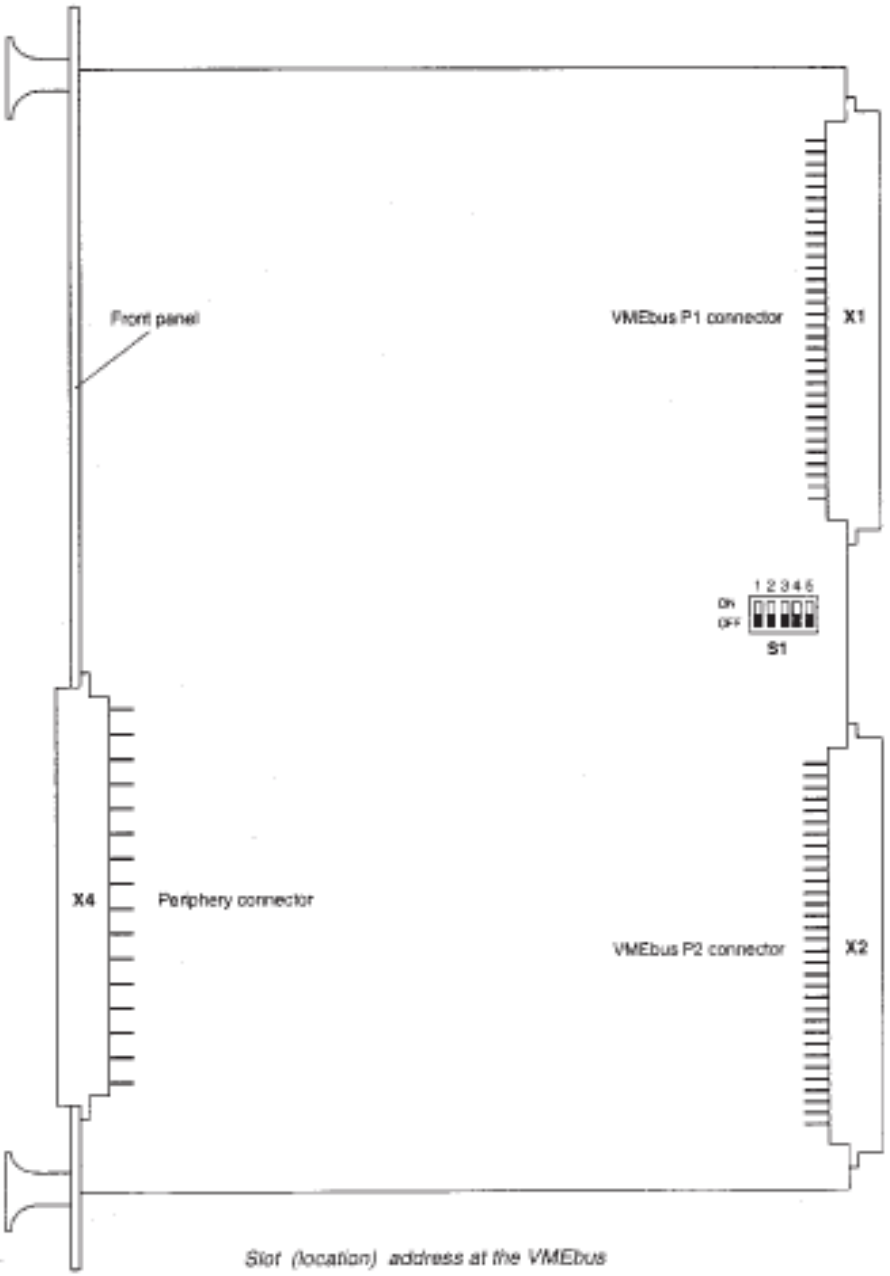
115	Input channel 0	*(AIN 0)*
117	Input channel 1	*(AIN 1)*
119	Input channel 2	*(AIN 2)*
121	Input channel 3	*(AIN 3)*
123	Input channel 4	*(AIN 4)*
125	Input channel 5	*(AIN 5)*
127	Input channel 6	*(AIN 6)*
129	Input channel 7	*(AIN 7)*
315	Output channel 0	*(AOUT 0)*
317	Output channel 1	*(AOUT 1)*
319	Output channel 2	*(AOUT 2)*
321	Output channel 3	*(AOUT 3)*
323	Output channel 4	*(AOUT 4)*
325	Output channel 5	*(AOUT 5)*
327	Output channel 6	*(AOUT 6)*
329	Output channel 7	*(AOUT 7)*
131, 331, 531	Reference points AGND for AINx , AOUTx and +/- 15 V supply	
338	Analog supply -15 V (de-coupled with 10 kΩ resistance)	
538	Analog supply +15 V (de-coupled with 10 kΩ resistance)	

Note: The measuring sockets are de-coupled from the input and/or output channels by de-coupling amplifiers and a 1-kΩ resistor.

LEDs lit when:

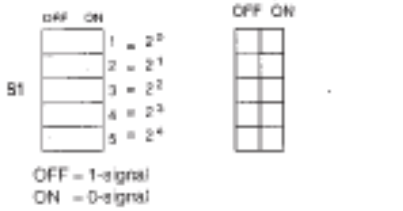
138A (red)	Analog supply +15 V is not provided
138B (red)	Analog supply -15 V is not provided
140 (green)	Output channels 0 to 3 enabled
240 (green)	Output channels 4 to 7 enabled

6 Assembly Diagram



Slot (location) address at the VMEbus

Example: address 18



OFF = 1-signal
ON = 0-signal

7 Use of the board

The following points must be observed for plant engineering when using the ADA 232:

- Wiring of the board
- Engineering with LogiCAD

7.1 Wiring of the board

When connecting the signal lines to the board inputs, care must be taken to ensure that the related signal wires (AIN+ with AIN- and AOUT with GND) are laid as twisted pairs!

Generally speaking, the plant wiring is carried out in such a manner that a pre-assembled connection unit - 48-pole connector with 2.2 m connection cable - and the following plug distributor (article No.: 029.209479) are located in the cubicle. The periphery is then connected to the plug connector.

7.2 Engineering with LogiCAD

With LogiCAD 3.1 for DPU, the ADA 232 is permanently linked via the ADA module in the I/O data chart.

Setting the output control (temporary / long-term saving), selecting the enabling for the output groups (internal/external) is carried out via the DPUKONF rack configurator.

When using the ADA 232 in a DPU under LogiCAD, synchronous mode (SYNC* synchronization signal available) is assumed.

8 Technical Specifications

POWER SUPPLY

• **VMEbus- processing and analog part**	UB5	=	+5 V, ±3%
	Itype	≤	1.2 A
	M5	=	Reference point (GND) of UB5

Note: *The supply for the analog part with ±15 V is generated via a DC/DC transformer which is fed UB5. The reference point of the analog part AGND is identical to GND.*

INPUTS

• **Analog inputs** *(differential inputs)*

Input voltage	Ue	=	+10 V...0 V... -10V
	Ue max.	=	±15 V
Input resistance	Re		≥500 kΩ
Overvoltage resistance *(common mode)*	Ue	=	200 V (max. 1s)

Note: *When Ue is overshot, the output values at the VMEbus remain constant (7FF0 H or 8000 H).*

Limit frequency	fg	=	1 kHz *(Above fg, the voltage reduction amounts to Ue = 40 dB/decade)*
Resolution			11 bit data plus sign
Relative conversion error			± 1LSB
Max. error *(total conversion area)*			± 5LSB
Conversion time	t	≤	40 µs (all channels)

1 LSB = 4.88 mV

OUTPUTS

• **Output channels** *(voltage outputs)*

	Ua	=	+10 V ... 0V ... -10 V
	Ia	≤	5 mA
Resolution			12 bits for the entire area
Conversion error	type		1LSB
Temperature error	type		0.05 LSB / °C
Conversion time	t	≤	10 µs for each channel

1 LSB = 4.88 mV

ENABLE INPUTS

Fext 0 ... Fext 1	Ue1	=	+12 V, to +29 V (= enable)
	Ie1	=	6 mA ± 30%
	Ue0	=	0 V to +5 V
	MFext 0 ... MFext 1	=	Reference point for Fext 0 ... Fext 1

AMBIENT CONDITIONS

Ambient temperature	0° to + 55° C (with natural convection)
Storage temperature	- 40° C to +85° C
Humidity	Class F

ELECTROMAGNETIC COMPATIBILITY (in the DPU subrack)

- Standard (pr) EN 50081-2 for emissions
- Standard (pr) EN 50082-2 for immunity

MECHANICAL DESIGN

- Format INTERMAS	
Size	6 - 04
Dimensions	ca. 233.4 mm x 160 mm x 20.5 mm (h x d x w)
- Connectors	
VMEbus P1	E96M-C1A, connectors X1
VMEbus P2	E96M-C1A, connectors X2
Periphery	E48M-C1A, connectors X4
Weight	approx. 500g

REORDER DATA

Type	ADA 232
Article-No.	029.202426